

MOS FIELD EFFECT TRANSISTOR

NP80N06CLC, NP80N06DLC, NP80N06ELC

SWITCHING

N-CHANNEL POWER MOS FET

INDUSTRIAL USE

DESCRIPTION

This product is N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Channel temperature 175 degree rated
- Super low on-state resistance
 $R_{DS(on)1} = 15 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 40 \text{ A)}$
 $R_{DS(on)2} = 20 \text{ m}\Omega \text{ MAX. (} V_{GS} = 5 \text{ V, } I_D = 23 \text{ A)}$
- Low C_{iss} : $C_{iss} = 2100 \text{ pF TYP.}$
- Built-in gate protection diode

ORDERING INFORMATION

PART NUMBER	PACKAGE
NP80N06CLC	TO-220AB
NP80N06DLC	TO-262
NP80N06ELC	TO-263

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0$)	V_{DSS}	60	V
Gate to Source Voltage ($V_{DS} = 0$)	V_{GSS}	± 20	V
Drain Current (DC) ^{Note1}	$I_{D(DC)}$	± 80	A
Drain Current (Pulse) ^{Note2}	$I_{D(pulse)}$	± 180	A
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_{T1}	1.8	W
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T2}	148	W
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +175	$^\circ\text{C}$
Single Avalanche Current ^{Note3}	I_{AS}	Figure 4	A
Single Avalanche Energy ^{Note3}	E_{AS}	Figure 4	mJ
Repetitive Avalanche Current ^{Note4}	I_{AR}	45	A
Repetitive Avalanche Energy ^{Note4}	E_{AR}	14.8	mJ

- Notes**
1. Package Limit = $\pm 75 \text{ A}$
 2. $PW \leq 10 \mu\text{s}$, Duty cycle $\leq 1 \%$
 3. Starting $T_{ch} = 25^\circ\text{C}$, $R_G = 25 \Omega$, $V_{GS} = 20 \text{ V} \rightarrow 0 \text{ V}$
 4. $T_{ch} \leq 175^\circ\text{C}$, $R_G = 25 \Omega$, $V_{GS} = 20 \text{ V} \rightarrow 0 \text{ V}$, Duty cycle $\leq 3\%$

THERMAL RESISTANCE

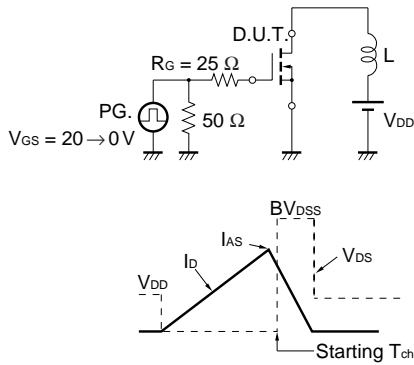
Channel to Case	$R_{th(ch-C)}$	1.01	$^\circ\text{C/W}$
Channel to Ambient	$R_{th(ch-A)}$	83.3	$^\circ\text{C/W}$

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 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

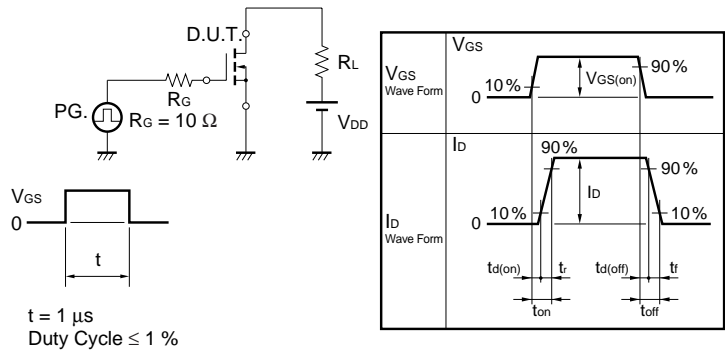
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 40 A		11	15	mΩ
	R _{DS(on)2}	V _{GS} = 5 V, I _D = 23 A		14	20	mΩ
	R _{DS(on)3}	V _{GS} = 4 V, I _D = 23 A		16	23	mΩ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.0	1.5	2.0	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 23 A	20	58		S
Drain Leakage Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0			10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0			±10	μA
Input Capacitance	C _{iSS}	V _{DS} = 10 V		2100	4600	pF
Output Capacitance	C _{oSS}	V _{GS} = 0		1100	1700	pF
Reverse Transfer Capacitance	C _{rSS}	f = 1 MHz		500	900	pF
Turn-on Delay Time	t _{d(on)}	I _D = 23 A		43	100	ns
Rise Time	t _r	V _{GS(on)} = 10 V		370	950	ns
Turn-off Delay Time	t _{d(off)}	V _{DD} = 30 V		320	640	ns
Fall Time	t _f	R _G = 10 Ω		320	800	ns
Total Gate Charge	Q _G	I _D = 45 A		100	150	nC
Gate to Source Charge	Q _{GS}	V _{DD} = 48 V		7.0		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = 10 V		40		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 23 A, V _{GS} = 0		1.0		V
Reverse Recovery Time	t _{rr}	I _F = 23A, V _{GS} = 0		100		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs		180		nC

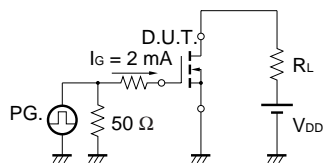
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



TYPICAL CHARACTERISTICS (T_A = 25 °C)

Figure 1. DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

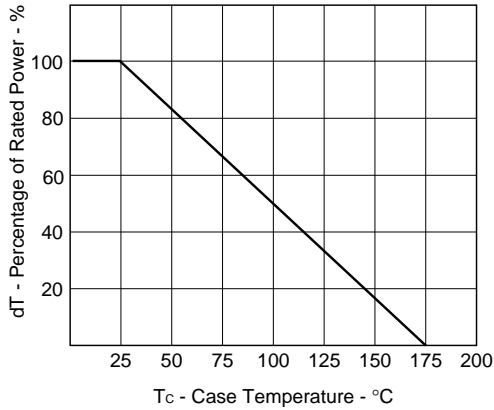


Figure 2. TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

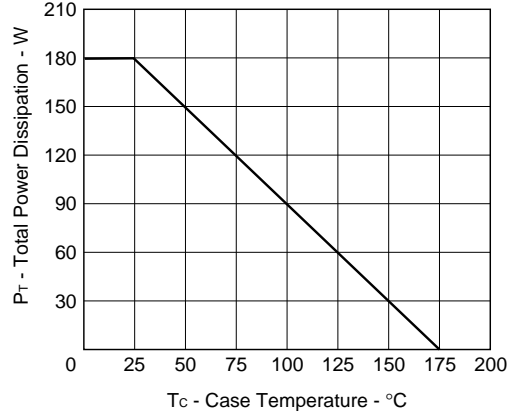


Figure 3. FORWARD BIAS SAFE OPERATING AREA

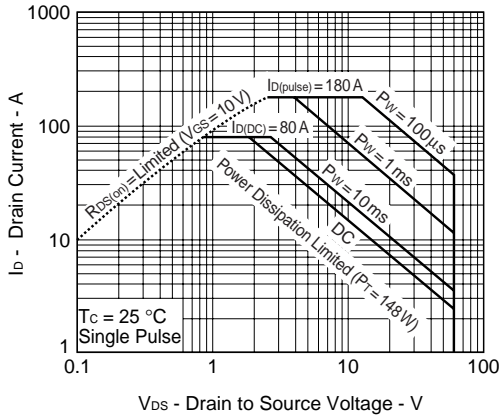


Figure 4. SINGLE AVALANCHE ENERGY DERATING FACTOR

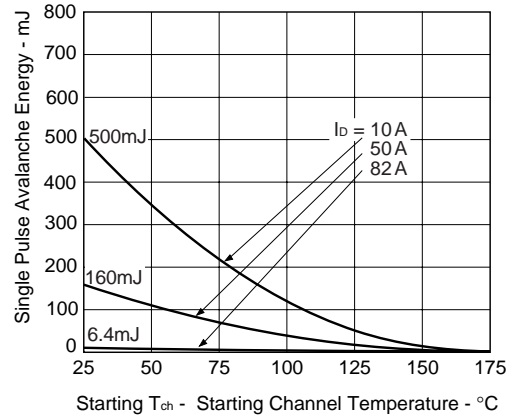


Figure 5. FORWARD TRANSFER CHARACTERISTICS

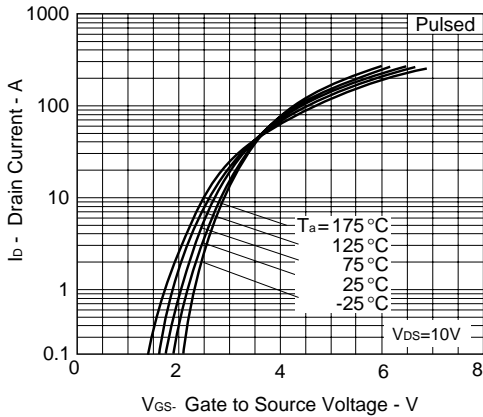


Figure 6. DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

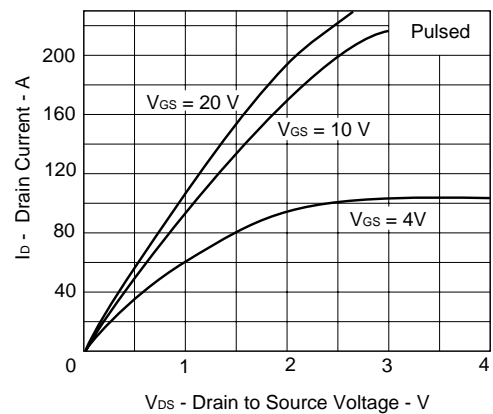


Figure 7. TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

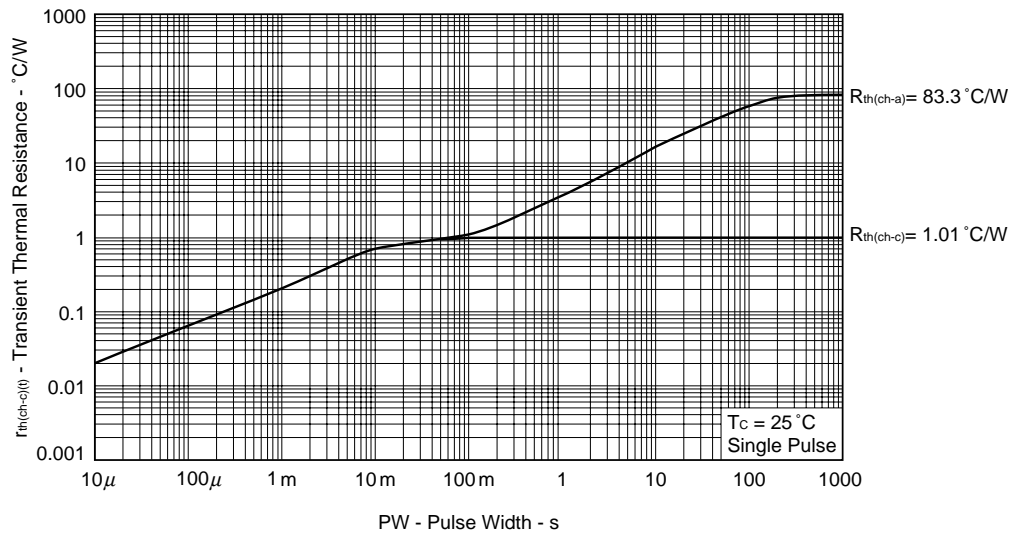


Figure 8. FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

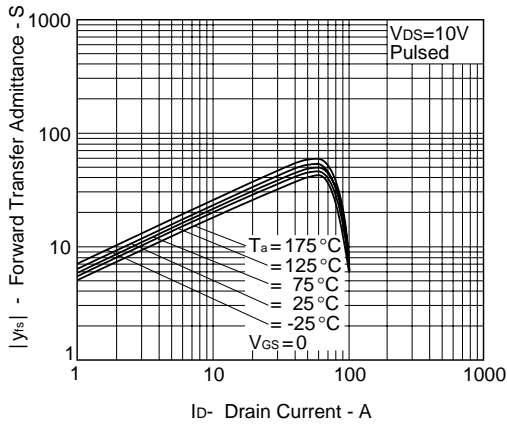


Figure 9. DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

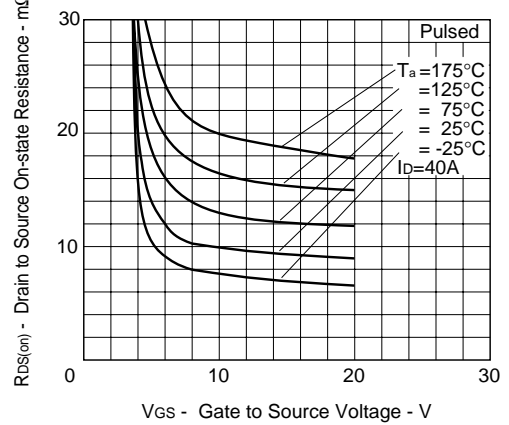


Figure 10. DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

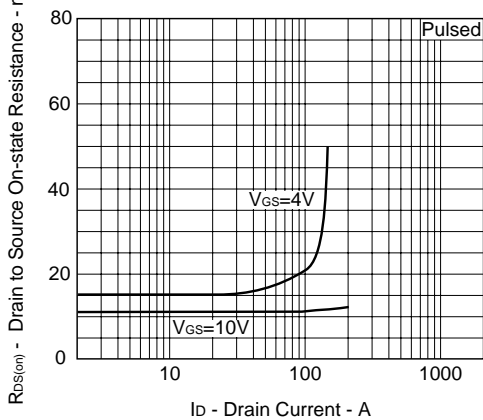


Figure 11. GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE

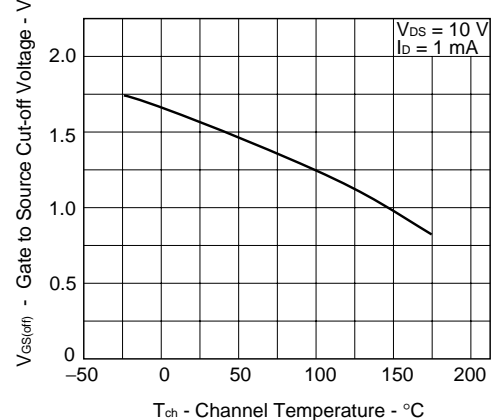


Figure 12. DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

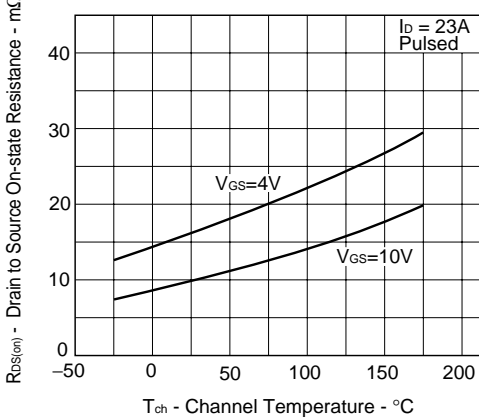


Figure 13. SOURCE TO DRAIN DIODE FORWARD VOLTAGE

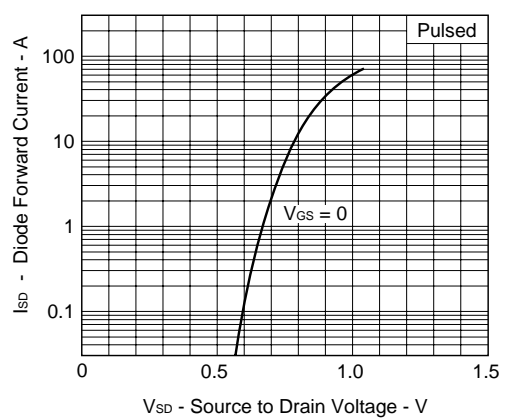


Figure 14. CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

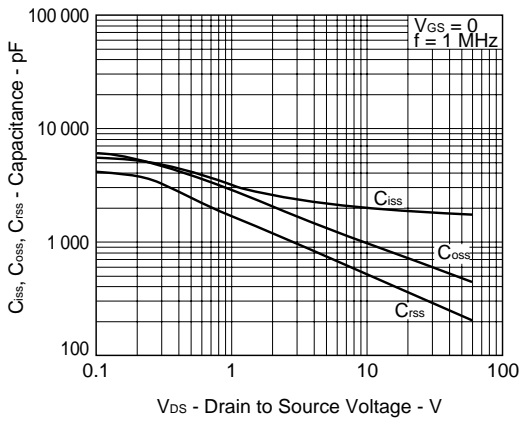


Figure 15. DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

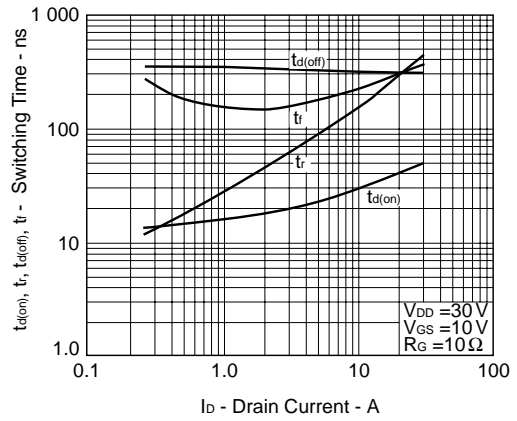


Figure 16. REVERSE RECOVERY TIME vs. DRAIN CURRENT

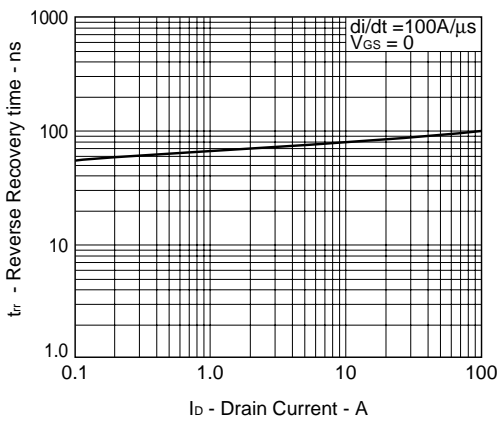
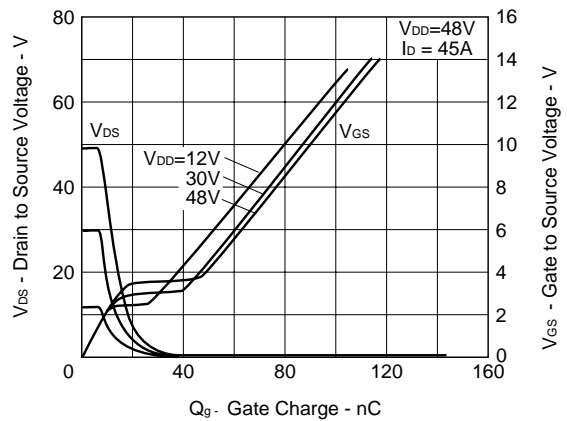
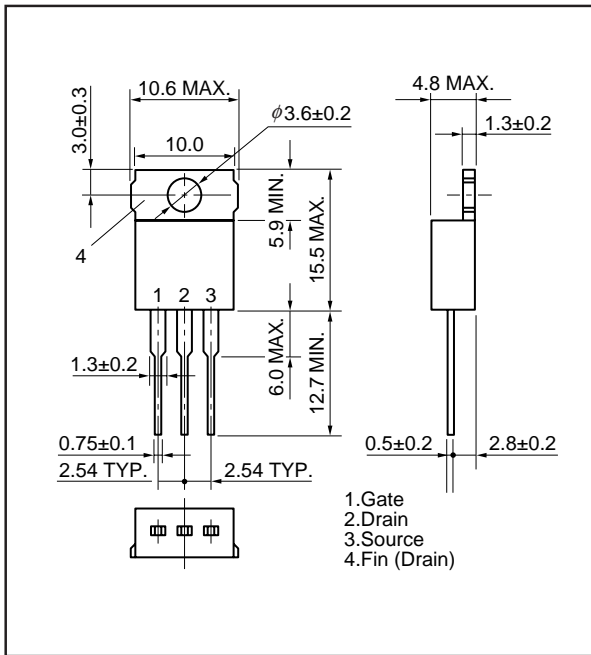


Figure 17. DYNAMIC INPUT/OUTPUT CHARACTERISTICS

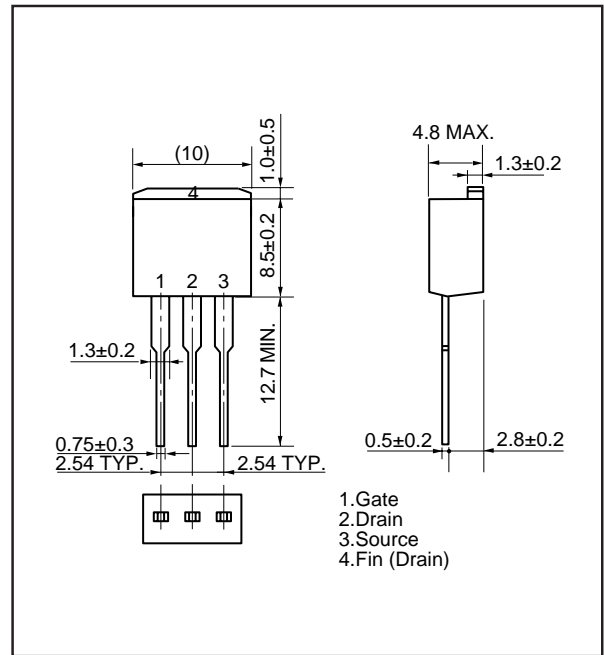


PACKAGE DRAWINGS (Unit: mm)

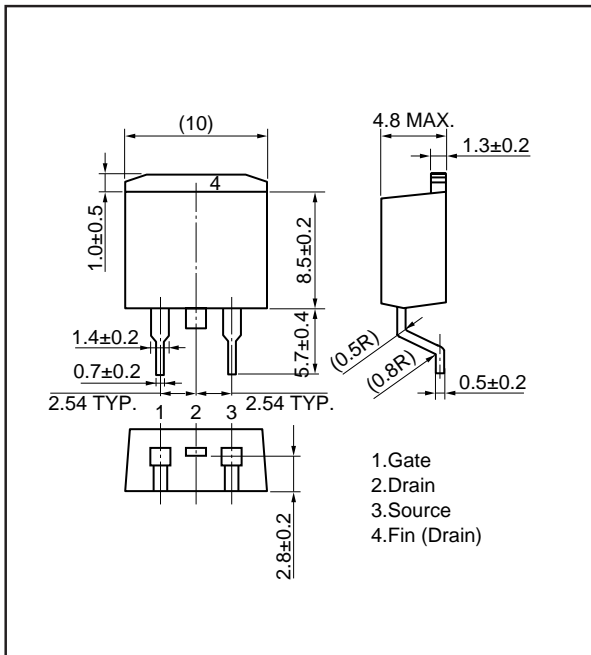
1) TO-220AB (MP-25)



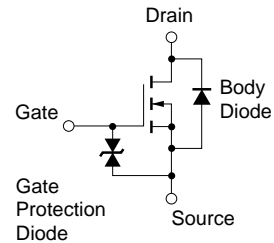
2) TO-262 (MP-25 Fin Cut)



3) TO-263 (MP-25ZJ)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

[MEMO]

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