DATA SHEET

NEC

MOS FIELD EFFECT TRANSISTOR

NP84N055CLE,NP84N055DLE,NP84N055ELE,NP84N055KLE

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

These products are N-channel MOS Field Effect Transistor designed for high current switching applications.

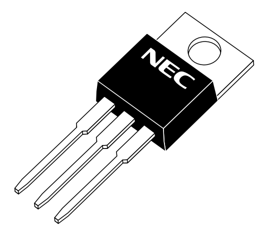
FEATURES

- Channel temperature 175 degree rated
- Super low on-state resistance
  $R_{DS(on)1}$ = 7.0 mΩ MAX. (V_{GS} = 10 V, I_D = 42 A)
  $R_{DS(on)2}$ = 8.7 mΩ MAX. (V_{GS} = 5 V, I_D = 42 A)
- Low C_{iss} : C_{iss} = 6130 pF TYP.
- Built-in gate protection diode

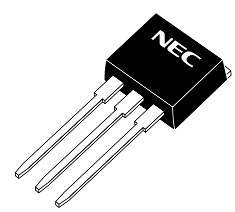
ORDERING INFORMATION

	PART NUMBER	PACKAGE
	NP84N055CLE	TO-220AB
	NP84N055DLE	TO-262
	NP84N055ELE	TO-263 (MP-25ZJ)
★	NP84N055KLE	TO-263 (MP-25ZK)

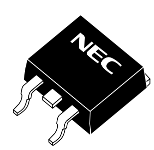
(TO-220AB)



(TO-262)



(TO-263)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	55	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C) Note1	$I_{D(DC)}$	±84	A
Drain Current (pulse) Note2	$I_{D(pulse)}$	±336	A
Total Power Dissipation (T_A = 25°C)	P_T	1.8	W
Total Power Dissipation (T_C = 25°C)	P_T	200	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to +175	°C
Single Avalanche Current Note3	I_{AS}	84 / 55 / 20	A
Single Avalanche Energy Note3	E_{AS}	70 / 302 / 400	mJ

Notes 1. Calculated constant current according to MAX. allowable channel temperature.

2. PW ≤ 10 μs, Duty cycle ≤ 1%

3. Starting T_{ch} = 25°C, V_{DD} = 28 V, R_G = 25 Ω , V_{GS} = 20 → 0 V (See Figure 4.)

THERMAL RESISTANCE

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	0.75	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	83.3	°C/W

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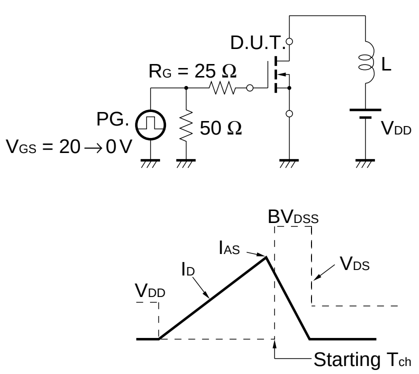
The mark ★ shows major revised points.

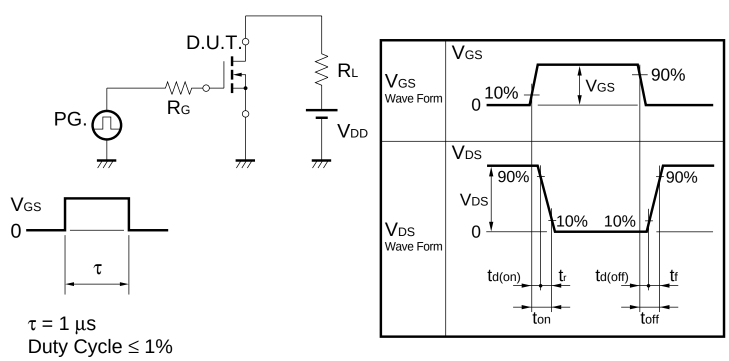
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 55 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1.5	2.0	2.5	V
Forward Transfer Admittance	$\| y_{fs} \|$	V_{DS} = 10 V, I_D = 42 A	27	58		S
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 42 A		5.6	7.0	mΩ
	$R_{DS(on)2}$	V_{GS} = 5 V, I_D = 42 A		6.5	8.7	mΩ
	$R_{DS(on)3}$	V_{GS} = 4.5 V, I_D = 42 A		7.0	9.4	mΩ
Input Capacitance	C_{iss}	V_{DS} = 25 V		6130	9200	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		710	1070	pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		350	630	pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 28 V, I_D = 42 A		29	64	ns
Rise Time	t_r	V_{GS} = 10 V		19	47	ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 1 Ω		120	230	ns
Fall Time	t_f			21	53	ns
Total Gate Charge 1	Q_{G1}	V_{DD} = 44 V, V_{GS} = 10 V, I_D = 84 A		120	180	nC
Total Gate Charge 2	Q_{G2}	V_{DD} = 44 V		65	98	nC
Gate to Source Charge	Q_{GS}	V_{GS} = 5 V		18		nC
Gate to Drain Charge	Q_{GD}	I_D = 84 A		33		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 84 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = 84 A, V_{GS} = 0 V		49		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		78		nC

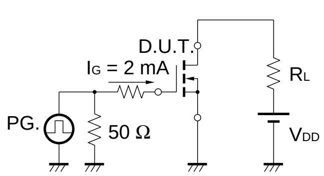
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



TYPICAL CHARACTERISTICS (T_A = 25°C)

Figure1. DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

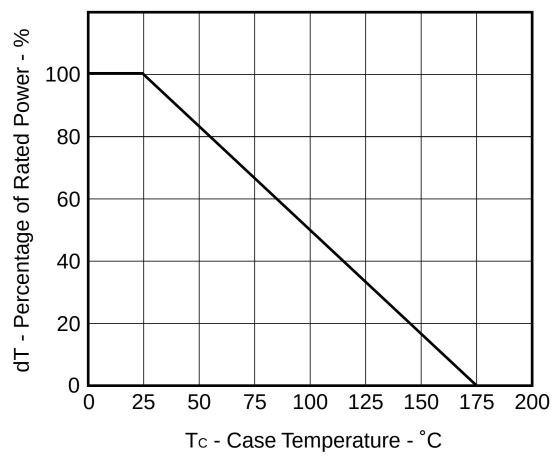


Figure2. TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

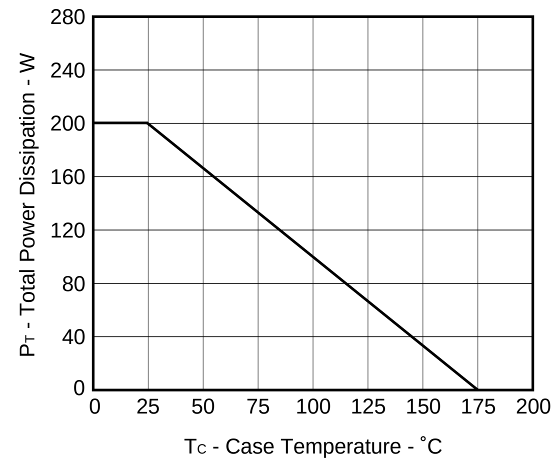


Figure3. FORWARD BIAS SAFE OPERATING AREA

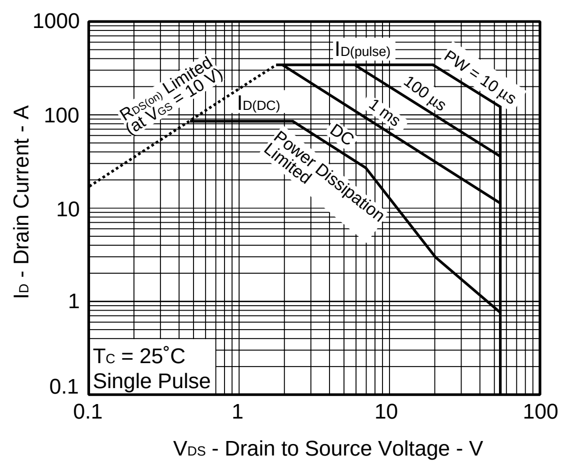


Figure4. SINGLE AVALANCHE ENERGY DERATING FACTOR

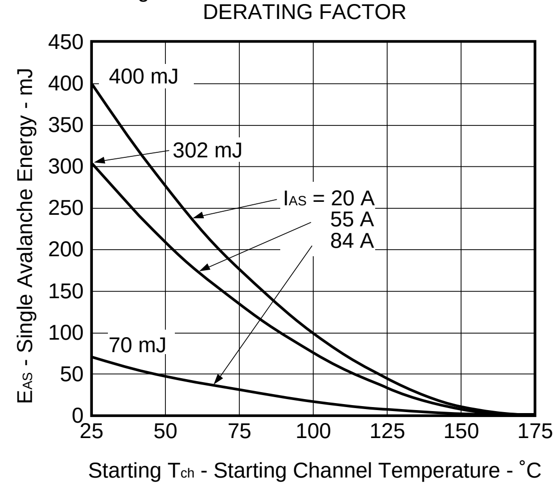


Figure5. TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

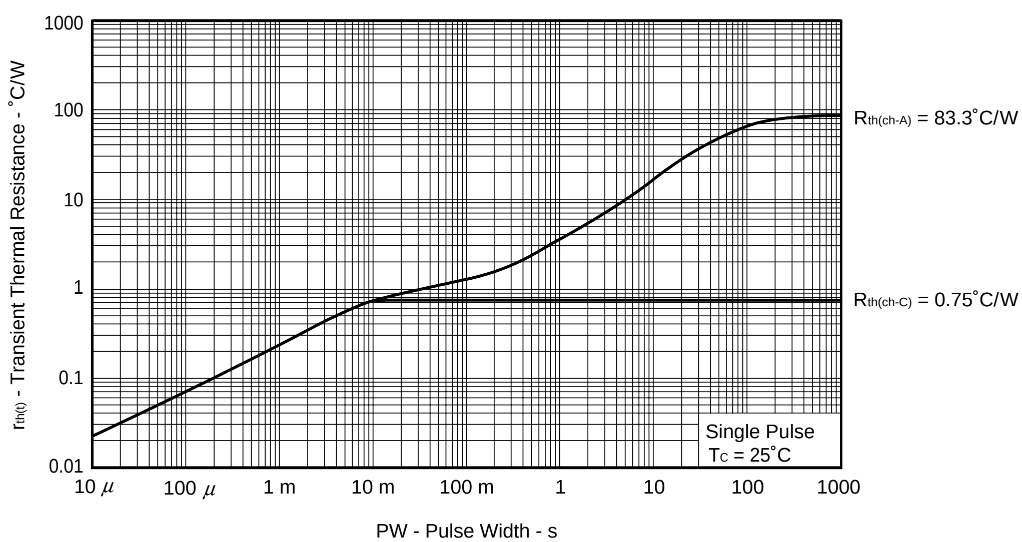


Figure6. FORWARD TRANSFER CHARACTERISTICS

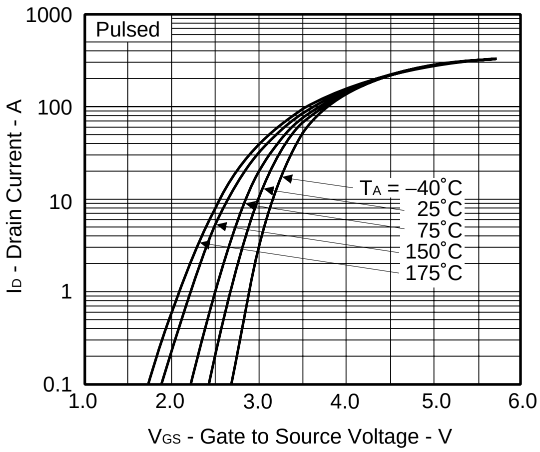


Figure7. DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

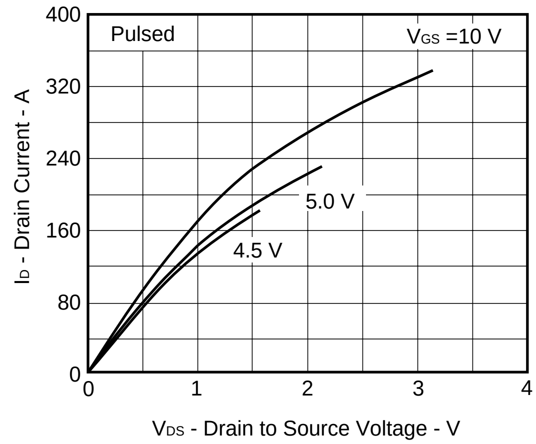


Figure8. FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

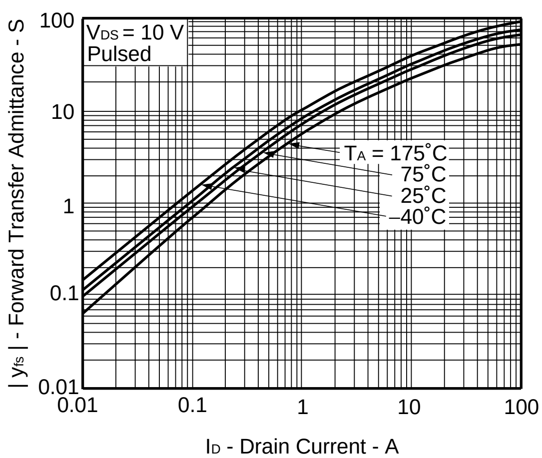


Figure9. DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

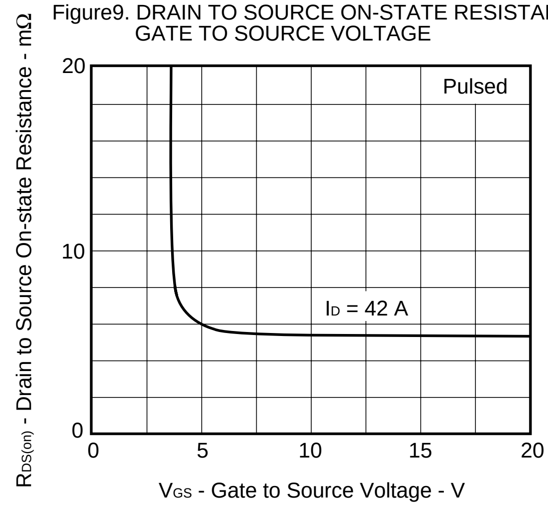


Figure10. DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

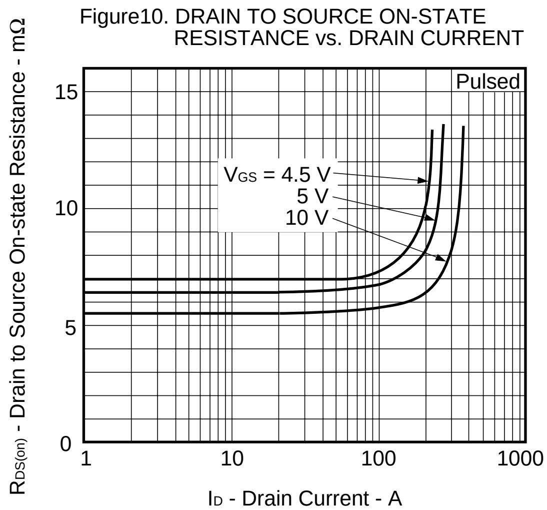


Figure11. GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

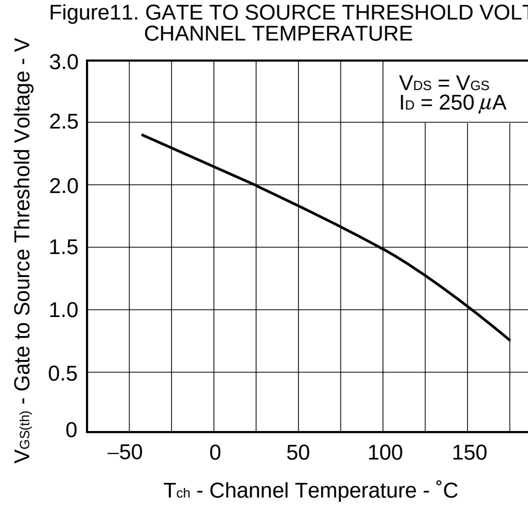


Figure12. DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

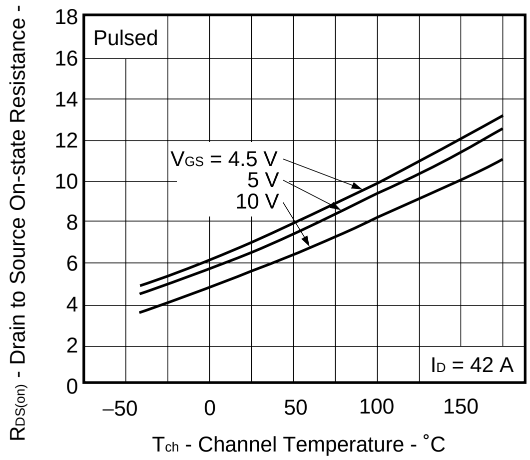


Figure13. SOURCE TO DRAIN DIODE FORWARD VOLTAGE

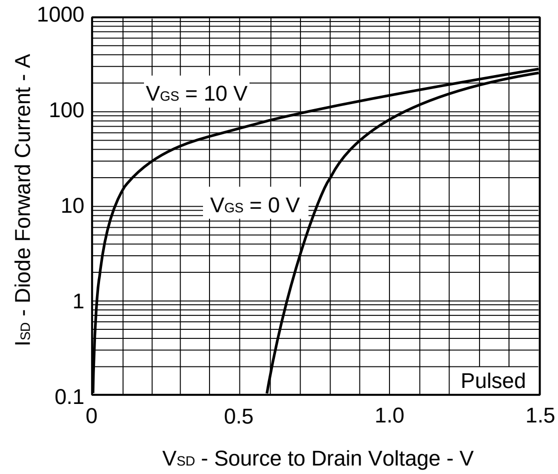


Figure14. CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

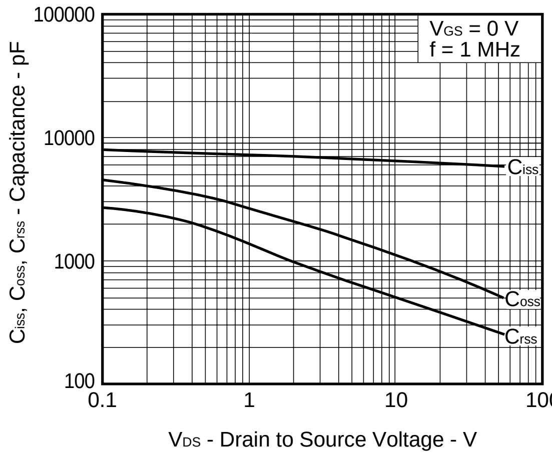


Figure15. SWITCHING CHARACTERISTICS

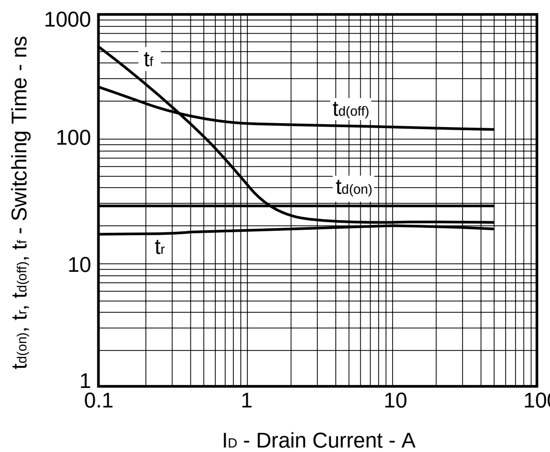


Figure16. REVERSE RECOVERY TIME vs. DRAIN CURRENT

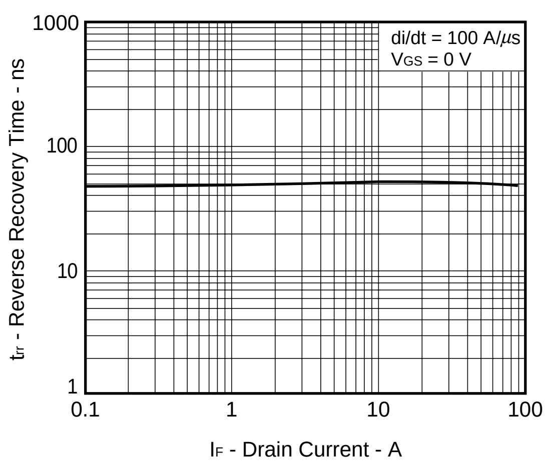
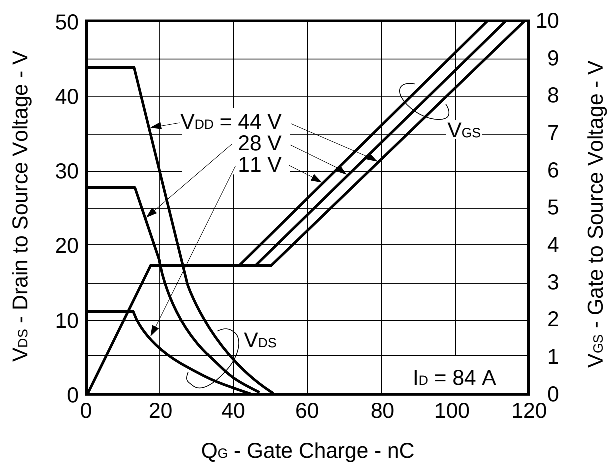
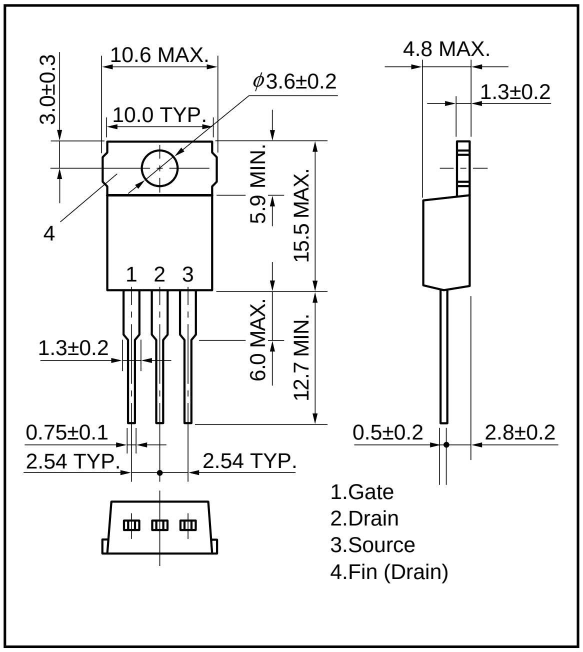


Figure17. DYNAMIC INPUT/OUTPUT CHARACTERISTICS

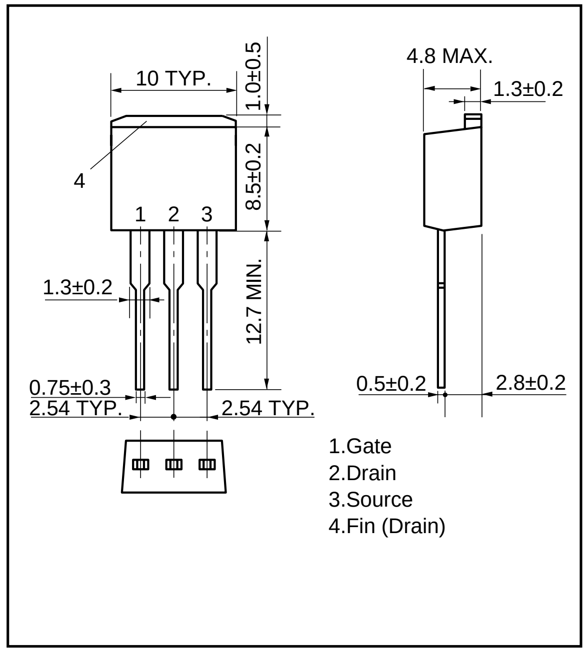


PACKAGE DRAWINGS (Unit: mm)

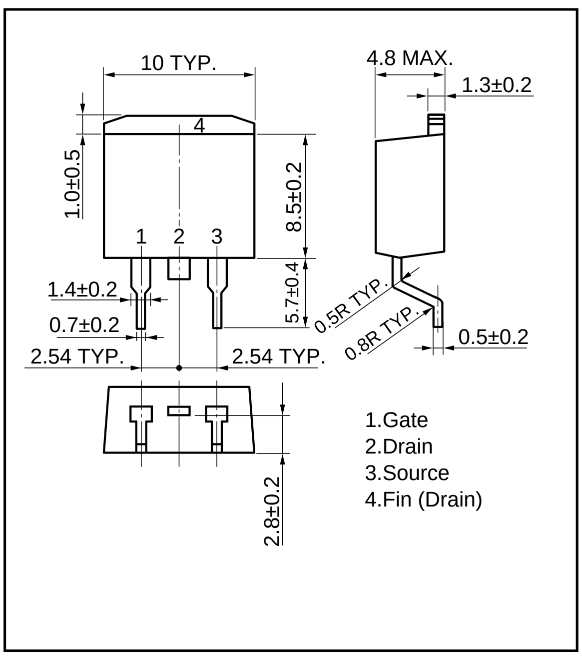
1) TO-220AB (MP-25)



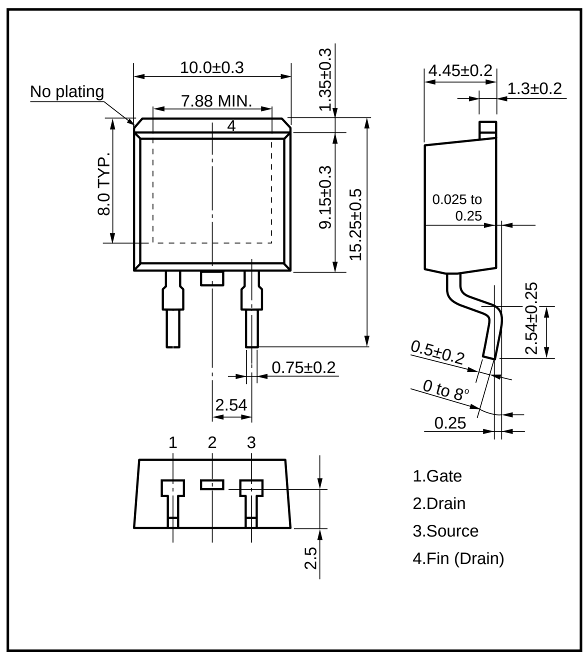
2) TO-262 (MP-25 Fin Cut)



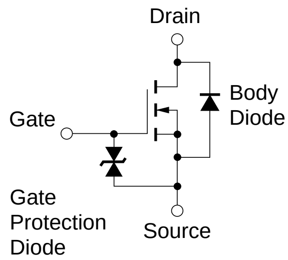
3) TO-263 (MP-25ZJ)



★ 4) TO-263 (MP-25ZK)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.