

NTD14N03R, NVD14N03R

Power MOSFET 14 Amps, 25 Volts

N-Channel DPAK

Features

- Planar HD3e Process for Fast Switching Performance
- Low $R_{DS(on)}$ to Minimize Conduction Loss
- Low C_{iss} to Minimize Driver Loss
- Low Gate Charge
- Optimized for High Side Switching Requirements in High-Efficiency DC-DC Converters
- NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Value | Unit |
|--|-----------------|------------|--------------------|
| Drain-to-Source Voltage | V_{DSS} | 25 | Vdc |
| Gate-to-Source Voltage – Continuous | V_{GS} | ± 20 | Vdc |
| Thermal Resistance – Junction-to-Case | $R_{\theta JC}$ | 6.0 | $^\circ\text{C/W}$ |
| Total Power Dissipation @ $T_A = 25^\circ\text{C}$ | P_D | 20.8 | W |
| Drain Current – Continuous @ $T_A = 25^\circ\text{C}$, Chip | I_D | 14 | A |
| – Continuous @ $T_A = 25^\circ\text{C}$, Limited by Package | I_D | 11.4 | A |
| – Single Pulse ($t_p \leq 10 \mu\text{s}$) | I_D | 28 | A |
| Thermal Resistance, Junction-to-Ambient (Note 1) | $R_{\theta JA}$ | 80 | $^\circ\text{C/W}$ |
| Total Power Dissipation @ $T_A = 25^\circ\text{C}$ | P_D | 1.56 | W |
| Drain Current – Continuous @ $T_A = 25^\circ\text{C}$ | I_D | 3.1 | A |
| Thermal Resistance, Junction-to-Ambient (Note 2) | $R_{\theta JA}$ | 120 | $^\circ\text{C/W}$ |
| Total Power Dissipation @ $T_A = 25^\circ\text{C}$ | P_D | 1.04 | W |
| Drain Current – Continuous @ $T_A = 25^\circ\text{C}$ | I_D | 2.5 | A |
| Operating and Storage Temperature Range | T_J, T_{stg} | -55 to 150 | $^\circ\text{C}$ |
| Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds | T_L | 260 | $^\circ\text{C}$ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. When surface mounted to an FR4 board using 0.5 sq. in pad size.
2. When surface mounted to an FR4 board using minimum recommended pad size.

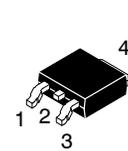
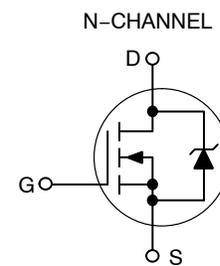


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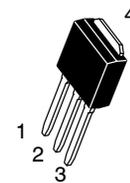
<http://onsemi.com>

14 AMPERES, 25 VOLTS

$R_{DS(on)} = 70.4 \text{ m}\Omega$ (Typ)

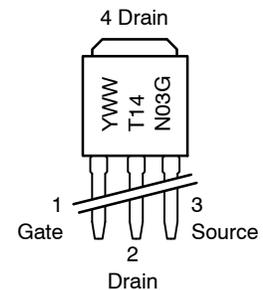
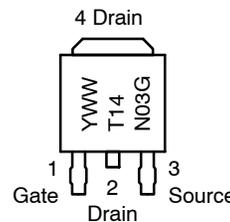


CASE 369C
DPAK
(Surface Mount)
STYLE 2



CASE 369D
DPAK-3
(Straight Lead)
STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENTS



Y = Year
WW = Work Week
14N03 = Device Code
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NTD14N03R, NVD14N03R

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

| Characteristics | Symbol | Min | Typ | Max | Unit |
|-----------------|--------|-----|-----|-----|------|
|-----------------|--------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | |
|---|----------------------|---------|---------|-----------|--------------|
| Drain-to-Source Breakdown Voltage (Note 3) (V _{GS} = 0 Vdc, I _D = 250 μAdc) Temperature Coefficient (Positive) | V _{(br)DSS} | 25 – | 28 – | – – | Vdc mV/°C |
| Zero Gate Voltage Drain Current (V _{DS} = 20 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 20 Vdc, V _{GS} = 0 Vdc, T _J = 150°C) | I _{DSS} | – – | – – | 1.0 10 | μAdc |
| Gate-Body Leakage Current (V _{GS} = ±20 Vdc, V _{DS} = 0 Vdc) | I _{GSS} | – | – | ±100 | nAdc |

ON CHARACTERISTICS (Note 3)

| | | | | | |
|--|---------------------|----------|-------------|-----------|--------------|
| Gate Threshold Voltage (Note 3) (V _{DS} = V _{GS} , I _D = 250 μAdc) Threshold Temperature Coefficient (Negative) | V _{GS(th)} | 1.0 – | 1.5 – | 2.0 – | Vdc mV/°C |
| Static Drain-to-Source On-Resistance (Note 3) (V _{GS} = 4.5 Vdc, I _D = 5 Adc) (V _{GS} = 10 Vdc, I _D = 5 Adc) | R _{DS(on)} | – – | 117 70.4 | 130 95 | mΩ |
| Forward Transconductance (Note 3) (V _{DS} = 10 Vdc, I _D = 5 Adc) | g _{FS} | – | 7.0 | – | Mhos |

DYNAMIC CHARACTERISTICS

| | | | | | | |
|----------------------|--|------------------|---|-----|---|----|
| Input Capacitance | (V _{DS} = 20 Vdc, V _{GS} = 0 V, f = 1 MHz) | C _{iss} | – | 115 | – | pF |
| Output Capacitance | | C _{oss} | – | 62 | – | |
| Transfer Capacitance | | C _{rss} | – | 33 | – | |

SWITCHING CHARACTERISTICS (Note 4)

| | | | | | | |
|---------------------|---|---------------------|-----|-----|---|----|
| Turn-On Delay Time | (V _{GS} = 10 Vdc, V _{DD} = 10 Vdc, I _D = 5 Adc, R _G = 3 Ω) | t _{d(on)} | – | 3.8 | – | ns |
| Rise Time | | t _r | – | 27 | – | |
| Turn-Off Delay Time | | t _{d(off)} | – | 9.6 | – | |
| Fall Time | | t _f | – | 2.0 | – | |
| Gate Charge | (V _{GS} = 5 Vdc, I _D = 5 Adc, V _{DS} = 10 Vdc) (Note 3) | Q _T | – | 1.8 | – | nC |
| | Q ₁ | – | 0.8 | – | | |
| | Q ₂ | – | 0.7 | – | | |

SOURCE-DRAIN DIODE CHARACTERISTICS

| | | | | | | |
|--------------------------------|---|-----------------|--------|--------------|----------|-----|
| Forward On-Voltage | (I _S = 5 Adc, V _{GS} = 0 Vdc) (Note 3) (I _S = 5 Adc, V _{GS} = 0 Vdc, T _J = 125°C) | V _{SD} | – – | 0.93 0.82 | 1.2 – | Vdc |
| Reverse Recovery Time | (I _S = 5 Adc, V _{GS} = 0 Vdc, di _S /dt = 100 A/μs) (Note 3) | t _{rr} | – | 6.6 | – | ns |
| | | t _a | – | 4.75 | – | |
| | | t _b | – | 1.88 | – | |
| Reverse Recovery Stored Charge | | Q _{RR} | – | 0.002 | – | μC |

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

NTD14N03R, NVD14N03R

TYPICAL CHARACTERISTICS

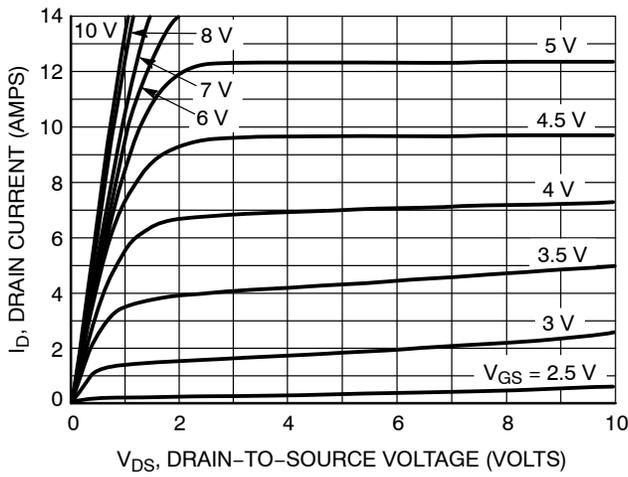


Figure 1. On-Region Characteristics

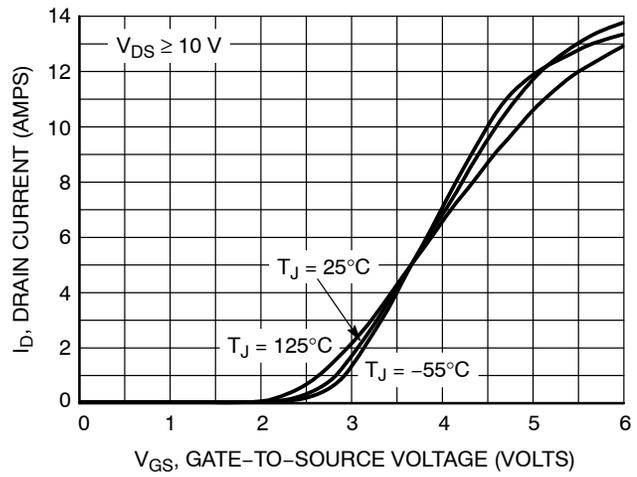


Figure 2. Transfer Characteristics

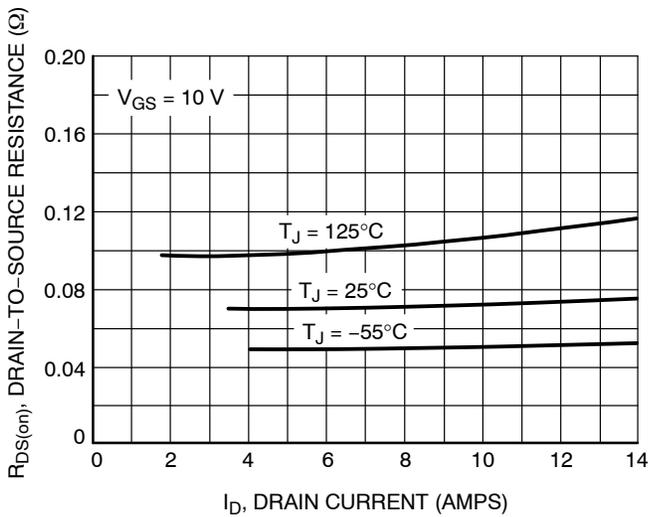


Figure 3. On-Resistance versus Drain Current and Temperature

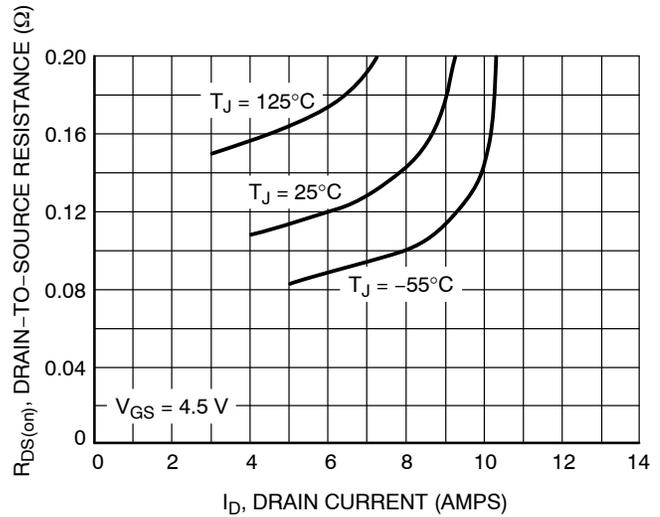


Figure 4. On-Resistance versus Drain Current and Temperature

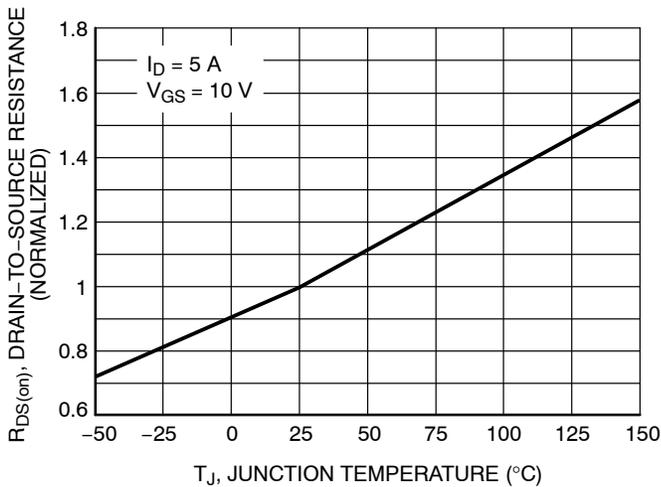


Figure 5. On-Resistance Variation with Temperature

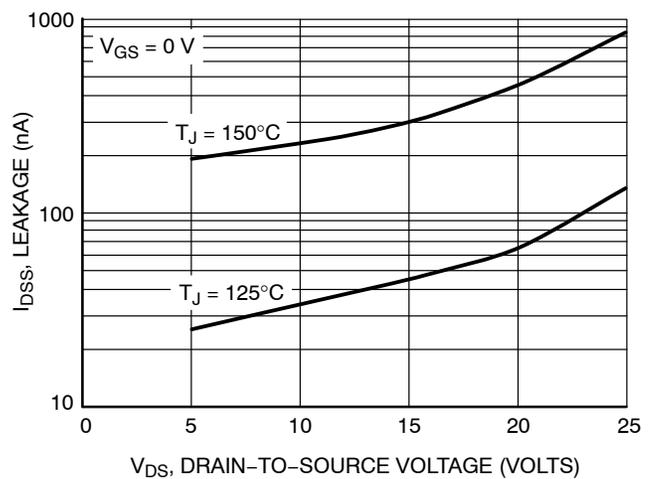


Figure 6. Drain-to-Source Leakage Current versus Voltage

NTD14N03R, NVD14N03R

TYPICAL CHARACTERISTICS

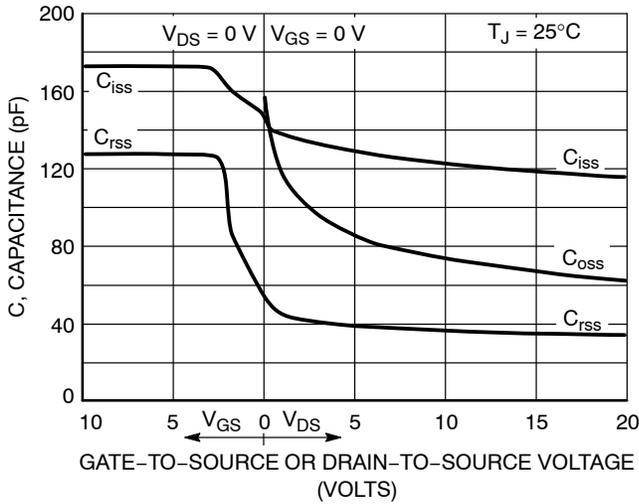


Figure 7. Capacitance Variation

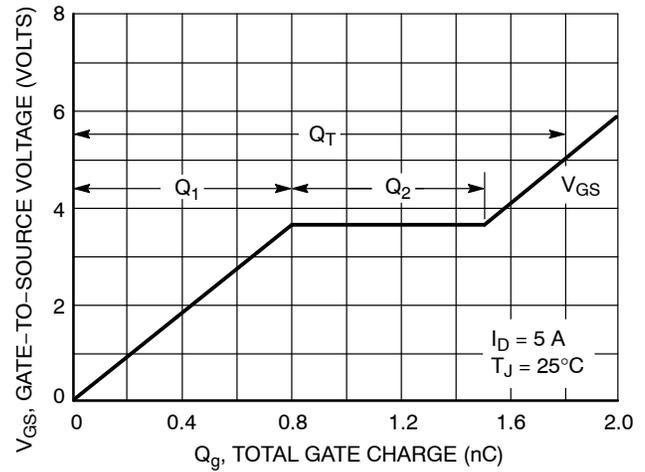


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

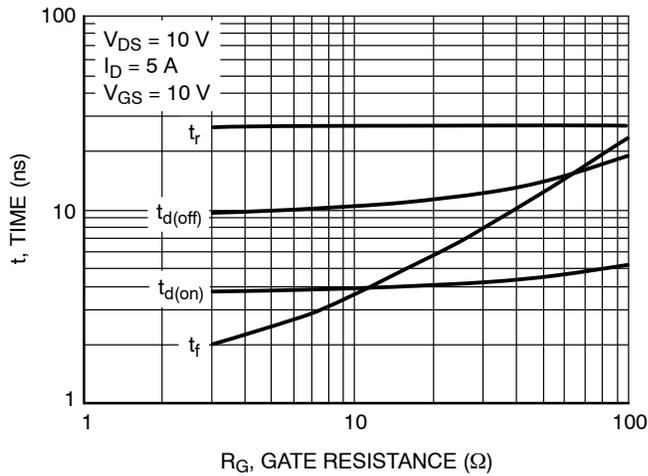


Figure 9. Resistive Switching Time Variation versus Gate Resistance

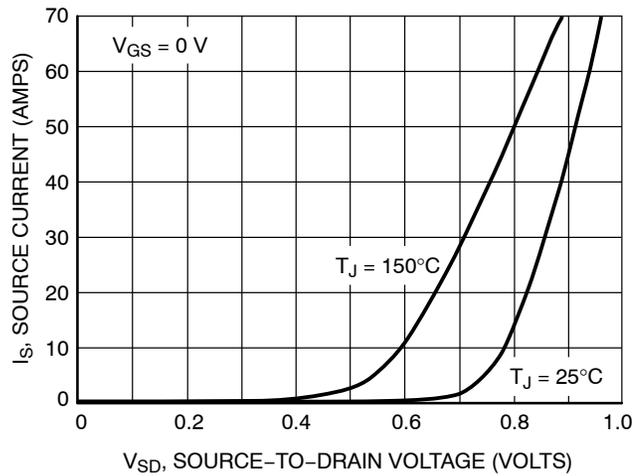


Figure 10. Diode Forward Voltage versus Current

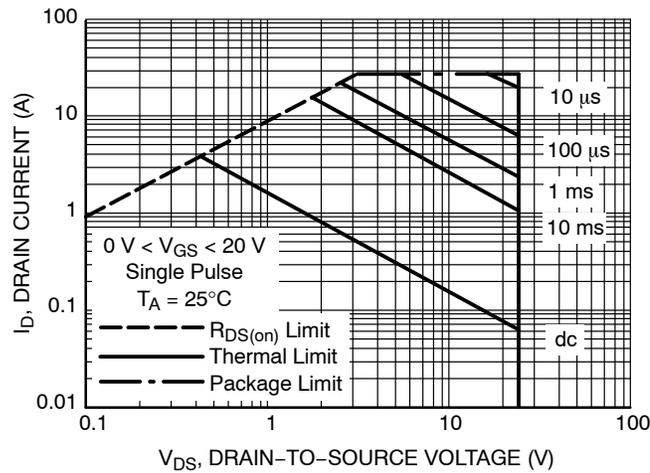


Figure 11. Maximum Rated Forward Biased Safe Operating Area

NTD14N03R, NVD14N03R

TYPICAL CHARACTERISTICS

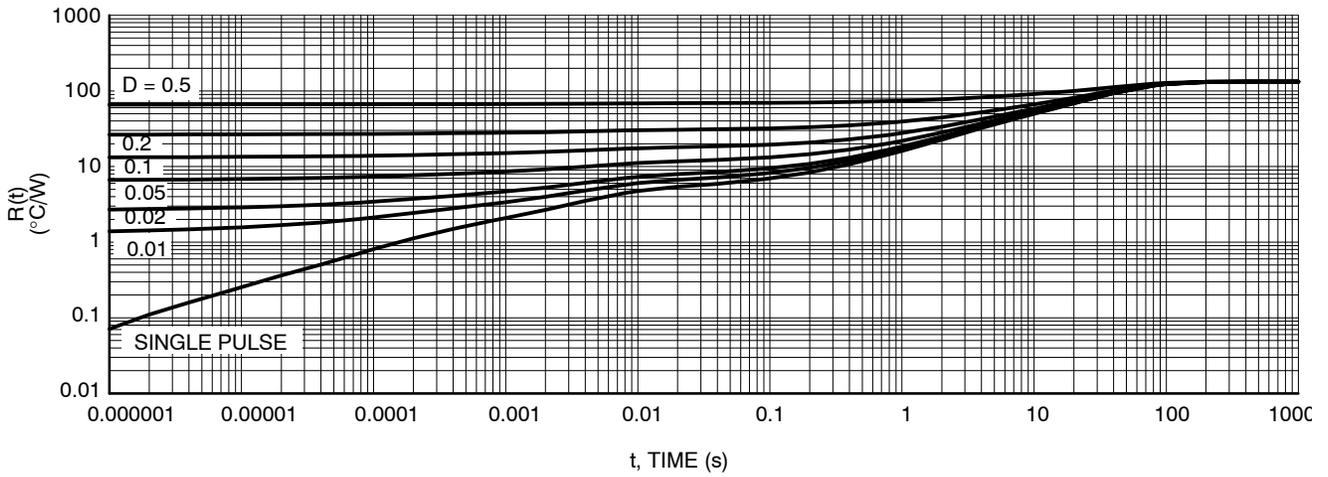


Figure 12. Thermal Response

ORDERING INFORMATION

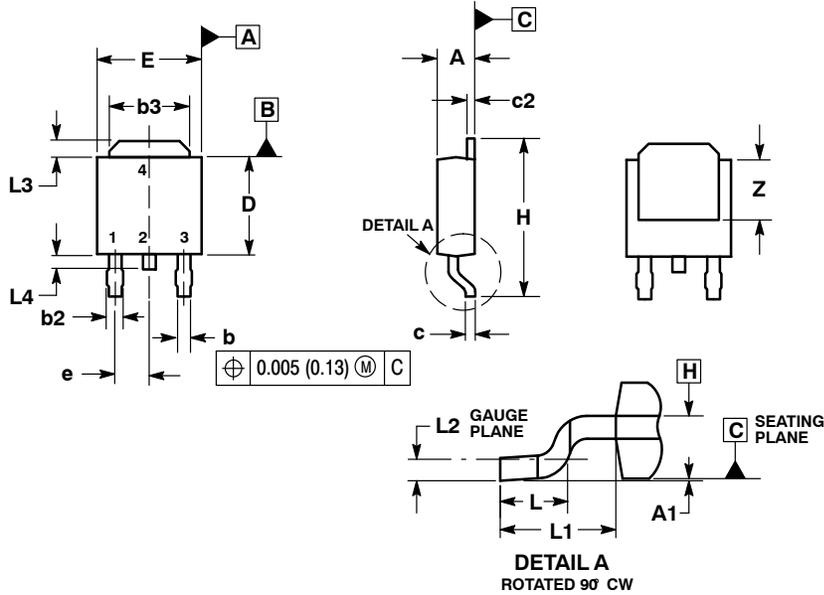
| Device | Package | Shipping† |
|--------------|-------------------|--------------------|
| NTD14N03RT4G | DPAK (Pb-Free) | 2500 / Tape & Reel |
| NVD14N03RT4G | DPAK (Pb-Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTD14N03R, NVD14N03R

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE) CASE 369C ISSUE D

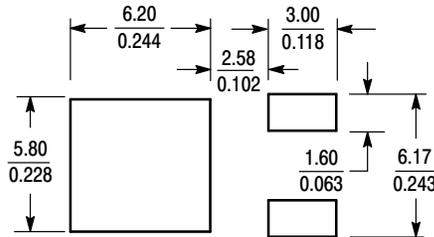


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.086 | 0.094 | 2.18 | 2.38 |
| A1 | 0.000 | 0.005 | 0.00 | 0.13 |
| b | 0.025 | 0.035 | 0.63 | 0.89 |
| b2 | 0.030 | 0.045 | 0.76 | 1.14 |
| b3 | 0.180 | 0.215 | 4.57 | 5.46 |
| c | 0.018 | 0.024 | 0.46 | 0.61 |
| c2 | 0.018 | 0.024 | 0.46 | 0.61 |
| D | 0.235 | 0.245 | 5.97 | 6.22 |
| E | 0.250 | 0.265 | 6.35 | 6.73 |
| e | 0.090 BSC | | 2.29 BSC | |
| H | 0.370 | 0.410 | 9.40 | 10.41 |
| L | 0.055 | 0.070 | 1.40 | 1.78 |
| L1 | 0.108 REF | | 2.74 REF | |
| L2 | 0.020 BSC | | 0.51 BSC | |
| L3 | 0.035 | 0.050 | 0.89 | 1.27 |
| L4 | --- | 0.040 | --- | 1.01 |
| Z | 0.155 | --- | 3.93 | --- |

SOLDERING FOOTPRINT*



SCALE 3:1 ($\frac{\text{mm}}{\text{inches}}$)

STYLE 2:

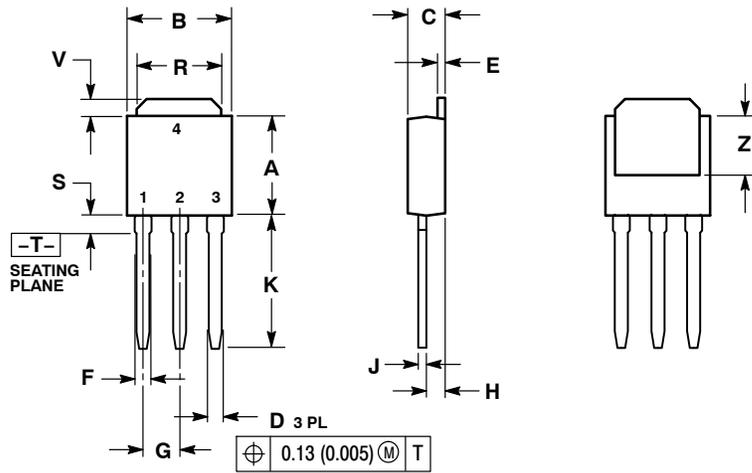
- PIN 1. GATE
- DRAIN
- SOURCE
- DRAIN

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTD14N03R, NVD14N03R

PACKAGE DIMENSIONS

IPAK CASE 369D ISSUE C



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.245 | 5.97 | 6.35 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.027 | 0.035 | 0.69 | 0.88 |
| E | 0.018 | 0.023 | 0.46 | 0.58 |
| F | 0.037 | 0.045 | 0.94 | 1.14 |
| G | 0.090 BSC | | 2.29 BSC | |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.350 | 0.380 | 8.89 | 9.65 |
| R | 0.180 | 0.215 | 4.45 | 5.45 |
| S | 0.025 | 0.040 | 0.63 | 1.01 |
| V | 0.035 | 0.050 | 0.89 | 1.27 |
| Z | 0.155 | --- | 3.93 | --- |

STYLE 2:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

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