

NTGD4161P

Power MOSFET

-30 V, -2.3 A, Dual P-Channel, TSOP-6

Features

- Fast Switching Speed
- Low Gate Charge
- Low $R_{DS(on)}$
- Independently Connected Devices to Provide Design Flexibility
- This is a Pb-Free Device

Applications

- Load Switch
- Battery Protection
- Portable Devices Like PDAs, Cellular Phones and Hard Drives

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	-30	V	
Gate-to-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	-2.1	A
		$T_A = 85^\circ\text{C}$	-1.5	
		$t \leq 5 \text{ s}$, $T_A = 25^\circ\text{C}$	-2.3	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	1.1	W
		$t \leq 5 \text{ s}$	1.3	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	-1.5	A
		$T_A = 85^\circ\text{C}$	-1.1	
Power Dissipation (Note 2)		$T_A = 25^\circ\text{C}$	0.6	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	I_{DM}	-10	A
Operating Junction and Storage Temperature	T_J , T_{STG}	-55 to 150	$^\circ\text{C}$	
Source Current (Body Diode)	I_S	-0.8	A	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	115	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - Steady State (Note 2)		225	
Junction-to-Ambient - $t \leq 5 \text{ s}$ (Note 1)		95	
Junction-to-Case - Steady State (Note 1)	$R_{\theta JC}$	40	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. When surface mounted to an FR4 board using 1 in. pad size (Cu. area = 1.2 in² [1 oz] including traces)
2. When surface mounted to an FR4 board using minimum recommended pad size (Cu. area = 0.047 in²)

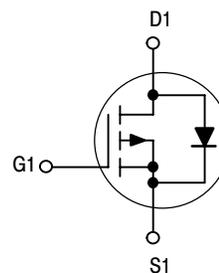


ON Semiconductor®

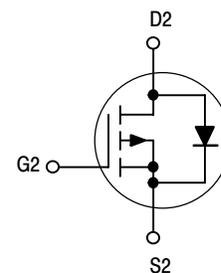
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ Max
-30 V	160 m Ω @ -10 V
	280 m Ω @ -4.5 V

P-Channel (MOSFET1)



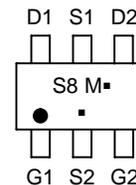
P-Channel (MOSFET2)



MARKING DIAGRAM



TSOP-6
CASE 318G
STYLE 13



S8 = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
NTGD4161PT1G	TSOP-6 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTGD4161P

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = -250 μA	-30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			22		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = -24 V	T _J = 25°C		-1.0	μA
			T _J = 125°C		-10	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = -250 μA	-1.0	-1.9	-3.0	V
Gate Threshold Temperature Coefficient	V _{GS(TH)} /T _J			-4.7		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = -10 V, I _D = -2.1 A		105	160	mΩ
		V _{GS} = -4.5 V, I _D = -1.6 A		190	280	
Forward Transconductance	g _{FS}	V _{DS} = -5.0 V, I _D = -2.1 A		2.7		S

CHARGES AND CAPACITANCES

Input Capacitance	C _{ISS}	V _{DS} = -15 V, f = 1.0 MHz, V _{GS} = 0 V		281		pF
Output Capacitance	C _{OSS}			50		
Reverse Transfer Capacitance	C _{RSS}			28		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = -10 V, V _{DS} = -5.0 V, I _D = -2.1 A		5.6	7.1	nC
Threshold Gate Charge	Q _{G(TH)}			0.65		
Gate-to-Source Charge	Q _{GS}			1.2		
Gate-to-Drain Charge	Q _{GD}			0.90		

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t _{d(on)}	V _{GS} = -4.5 V, V _{DD} = -15 V, I _D = -1.0 A, R _G = 6.0 Ω		7.6	14	ns
Rise Time	t _r			9.2	23	
Turn-Off Delay Time	t _{d(off)}			12.5	20	
Fall Time	t _f			4.5	12	

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = -0.8 A	T _J = 25°C		-0.79	-1.2	V
			T _J = 125°C		-0.65		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = -0.8 A		8.0		ns	
Charge Time	t _a			5.7			
Discharge Time	t _b			2.3			
Reverse Recovery Charge	Q _{RR}			3			nC

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

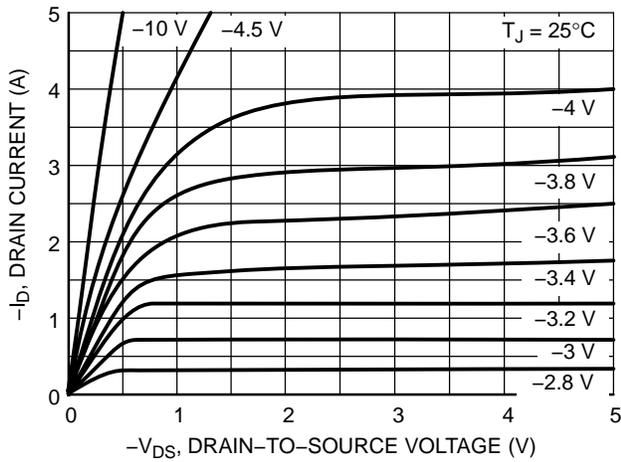


Figure 1. On-Region Characteristics

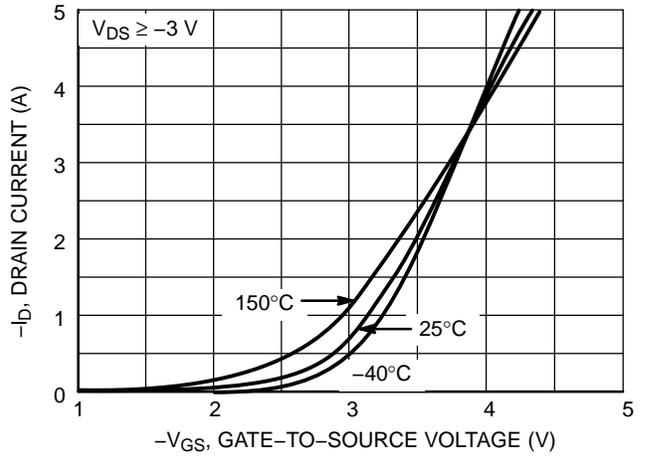


Figure 2. Transfer Characteristics

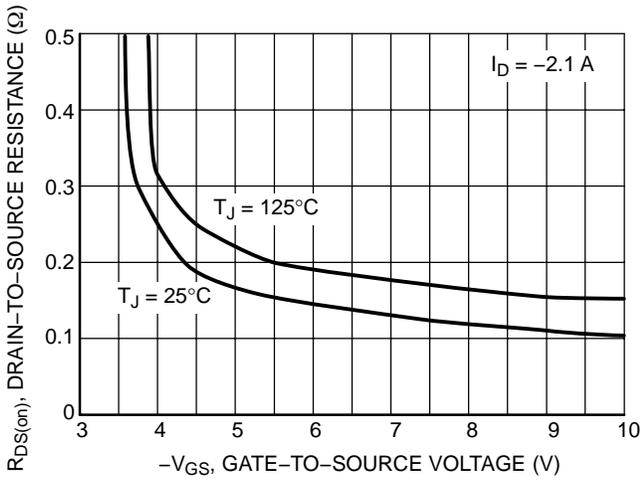


Figure 3. On-Resistance versus Gate-to-Source Voltage

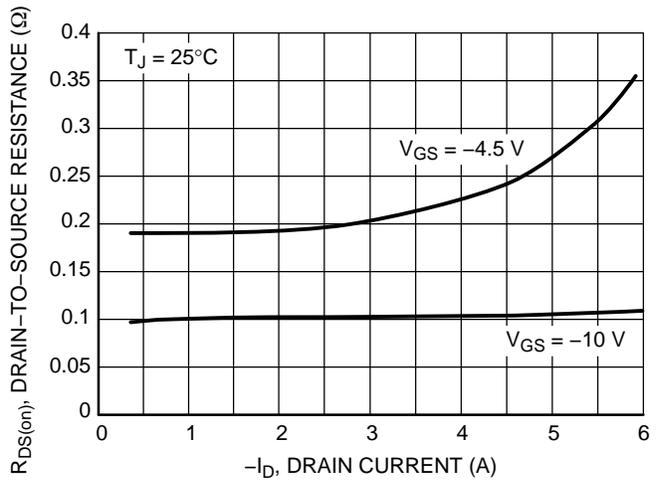


Figure 4. On-Resistance versus Drain Current and Temperature

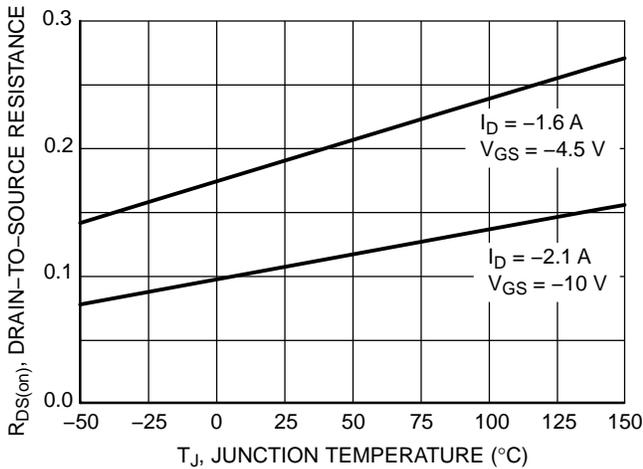


Figure 5. On-Resistance Variation with Temperature

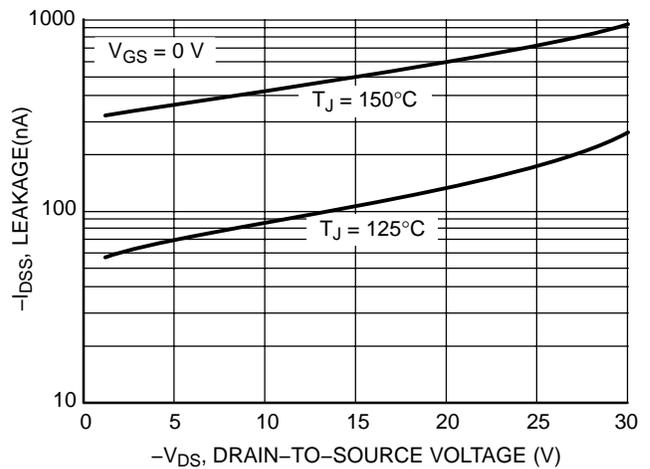


Figure 6. On-Resistance Variation with Temperature

NTGD4161P

TYPICAL PERFORMANCE CURVES

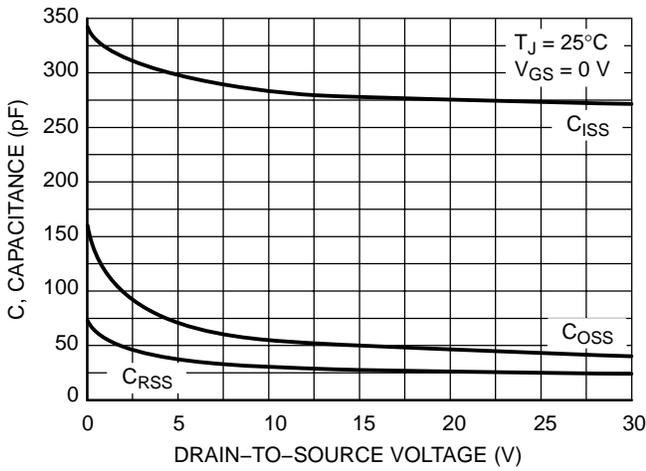


Figure 7. Capacitance Variation

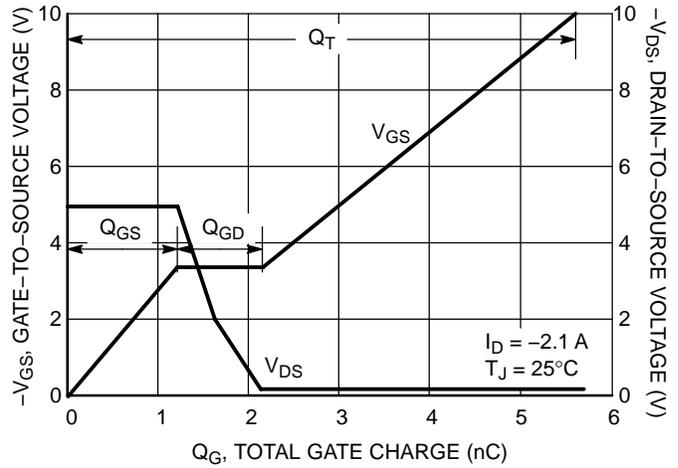


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

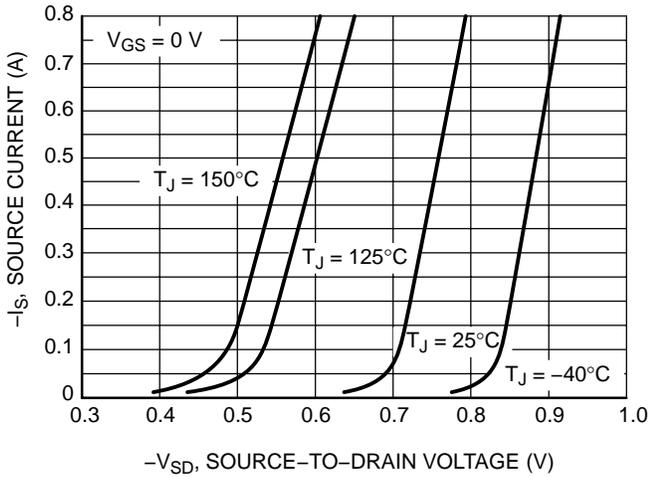


Figure 9. Diode Forward Voltage versus Current

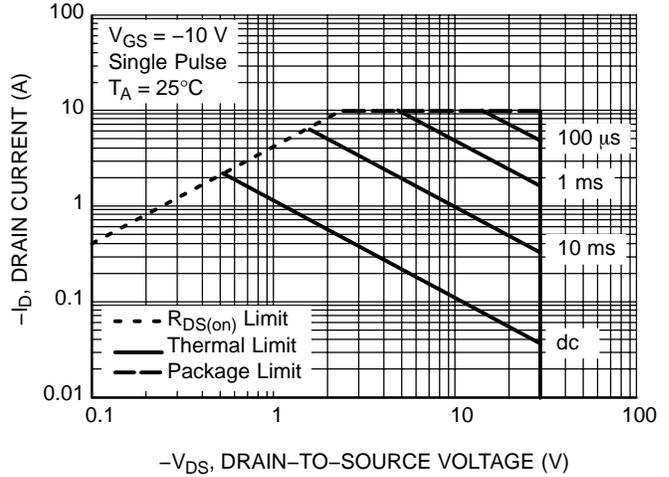


Figure 10. Maximum Rated Forward Biased Safe Operating Area

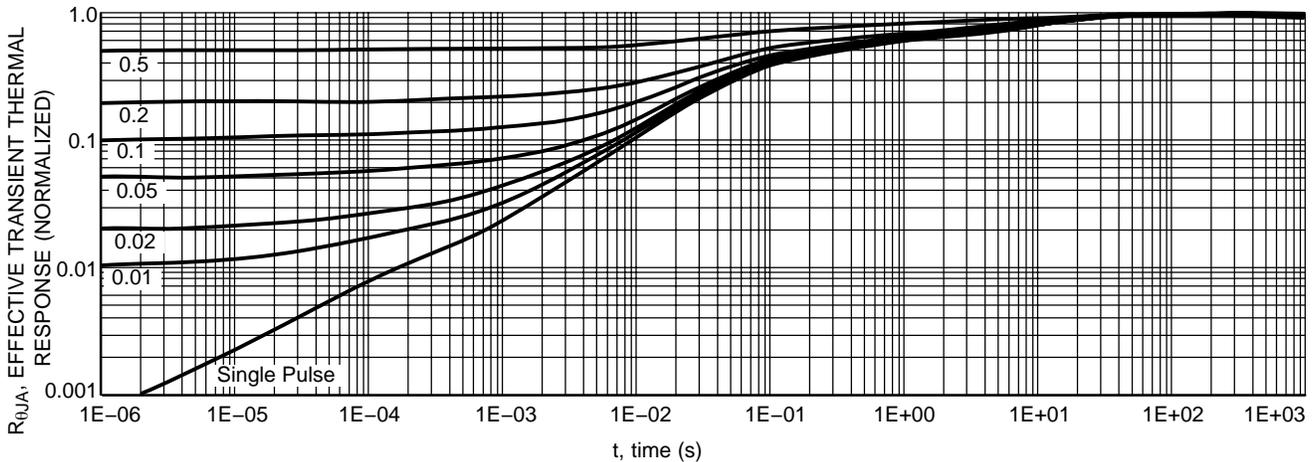
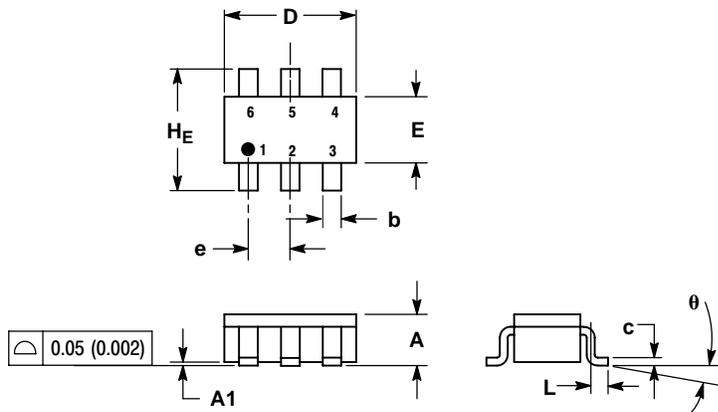


Figure 11. FET Thermal Response

NTGD4161P

PACKAGE DIMENSIONS

TSOP-6 CASE 318G-02 ISSUE S



NOTES:

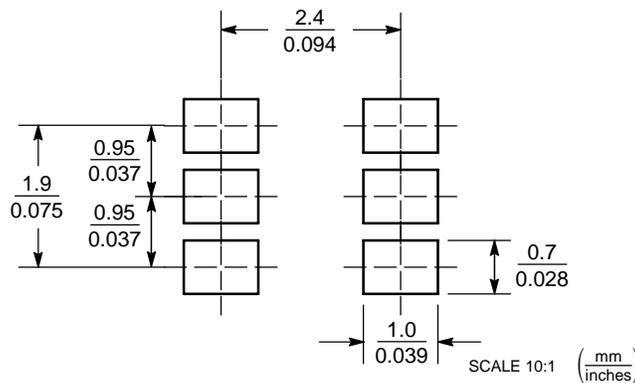
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.38	0.50	0.010	0.014	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
HE	2.50	2.75	3.00	0.099	0.108	0.118
theta	0°	-	10°	0°	-	10°

STYLE 13:

- PIN 1. GATE 1
- SOURCE 2
- GATE 2
- DRAIN 2
- SOURCE 1
- DRAIN 1

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative