

# DATA SHEET

## **PDTA124E series**

**PNP resistor-equipped transistors;**

**R1 = 22 k $\Omega$ , R2 = 22 k $\Omega$**

Product specification  
Supersedes data of 2001 Jun 11

2003 Apr 14

## PNP resistor-equipped transistors; R1 = 22 k $\Omega$ , R2 = 22 k $\Omega$

## PDTA124E series

### FEATURES

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

### APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V <sub>CEO</sub>	collector-emitter voltage	–	–50	V
I <sub>O</sub>	output current (DC)	–	–100	mA
R1	bias resistor	22	–	k $\Omega$
R2	bias resistor	22	–	k $\Omega$

### DESCRIPTION

PNP resistor-equipped transistor (see “Simplified outline, symbol and pinning” for package details).

### PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	NPN COMPLEMENT
	PHILIPS	EIAJ		
PDTA124EE	SOT416	SC-75	05	PDTC124EE
PDTA124EEF	SOT490	SC-89	3R	PDTC124EEF
PDTA124EK	SOT346	SC-59	05	PDTC124EK
PDTA124EM	SOT883	SC-101	DH	PDTC124EM
PDTA124ES	SOT54 (TO-92)	SC-43	TA124E	PDTC124ES
PDTA124ET	SOT23	–	*05 <sup>(1)</sup>	PDTC124ET
PDTA124EU	SOT323	SC-70	*05 <sup>(1)</sup>	PDTC124EU

### Note

1. \* = p: Made in Hong Kong.  
\* = t: Made in Malaysia.  
\* = W: Made in China.

PNP resistor-equipped transistors;  
 R1 = 22 kΩ, R2 = 22 kΩ

PDTA124E series

SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PDTA124ES	<p>MAM338</p>	1 2 3	base collector emitter
PDTA124EE PDTA124EEF PDTA124EK PDTA124ET PDTA124EU	<p>Top view</p> <p>MDB271</p>	1 2 3	base emitter collector
PDTA124EM	<p>Bottom view</p> <p>MDB267</p>	1 2 3	base emitter collector

PNP resistor-equipped transistors;  
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## PDTA124E series

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CBO</sub>	collector-base voltage	open emitter	–	–50	V
V <sub>CEO</sub>	collector-emitter voltage	open base	–	–50	V
V <sub>EBO</sub>	emitter-base voltage	open collector	–	–10	V
V <sub>I</sub>	input voltage positive negative		–	+10	V
			–	–40	V
I <sub>O</sub>	output current (DC)		–	–100	mA
I <sub>CM</sub>	peak collector current		–	–100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C			
	SOT54	note 1	–	500	mW
	SOT23	note 1	–	250	mW
	SOT346	note 1	–	250	mW
	SOT323	note 1	–	200	mW
	SOT416	note 1	–	150	mW
	SOT490	notes 1 and 2	–	250	mW
SOT883	notes 2 and 3	–	250	mW	
T <sub>stg</sub>	storage temperature		–65	+150	°C
T <sub>j</sub>	junction temperature		–	150	°C
T <sub>amb</sub>	operating ambient temperature		–65	+150	°C

**Notes**

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60  $\mu$ m copper strip line.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th j-a</sub>	thermal resistance from junction to ambient	in free air		
	SOT54	note 1	250	K/W
	SOT23	note 1	500	K/W
	SOT346	note 1	500	K/W
	SOT323	note 1	625	K/W
	SOT416	note 1	833	K/W
	SOT490	notes 1 and 2	500	K/W
SOT883	notes 2 and 3	500	K/W	

**Notes**

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2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60  $\mu$ m copper strip line.

PNP resistor-equipped transistors;  
 $R1 = 22 \text{ k}\Omega$ ,  $R2 = 22 \text{ k}\Omega$

PDTA124E series

### CHARACTERISTICS

$T_{\text{amb}} = 25 \text{ }^\circ\text{C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{\text{CBO}}$	collector-base cut-off current	$V_{\text{CB}} = -50 \text{ V}$ ; $I_{\text{E}} = 0$	–	–	–100	nA
$I_{\text{CEO}}$	collector-emitter cut-off current	$V_{\text{CE}} = -30 \text{ V}$ ; $I_{\text{B}} = 0$	–	–	–1	$\mu\text{A}$
		$V_{\text{CE}} = -30 \text{ V}$ ; $I_{\text{B}} = 0$ ; $T_{\text{j}} = 150 \text{ }^\circ\text{C}$	–	–	–50	$\mu\text{A}$
$I_{\text{EBO}}$	emitter-base cut-off current	$V_{\text{EB}} = -5 \text{ V}$ ; $I_{\text{C}} = 0$	–	–	–180	$\mu\text{A}$
$h_{\text{FE}}$	DC current gain	$V_{\text{CE}} = -5 \text{ V}$ ; $I_{\text{C}} = -5 \text{ mA}$	60	–	–	
$V_{\text{CEsat}}$	collector-emitter saturation voltage	$I_{\text{C}} = -10 \text{ mA}$ ; $I_{\text{B}} = -0.5 \text{ mA}$	–	–	–150	mV
$V_{\text{i(off)}}$	input-off voltage	$I_{\text{C}} = -100 \text{ }\mu\text{A}$ ; $V_{\text{CE}} = -5 \text{ V}$	–	–1.1	–0.8	V
$V_{\text{i(on)}}$	input-on voltage	$I_{\text{C}} = -5 \text{ mA}$ ; $V_{\text{CE}} = -0.3 \text{ V}$	–2.5	–1.7	–	V
R1	input resistor		15.4	22	28.6	$\text{k}\Omega$
$\frac{R2}{R1}$	resistor ratio		0.8	1	1.2	
$C_{\text{c}}$	collector capacitance	$I_{\text{E}} = i_{\text{e}} = 0$ ; $V_{\text{CB}} = -10 \text{ V}$ ; $f = 1 \text{ MHz}$	–	–	3	pF

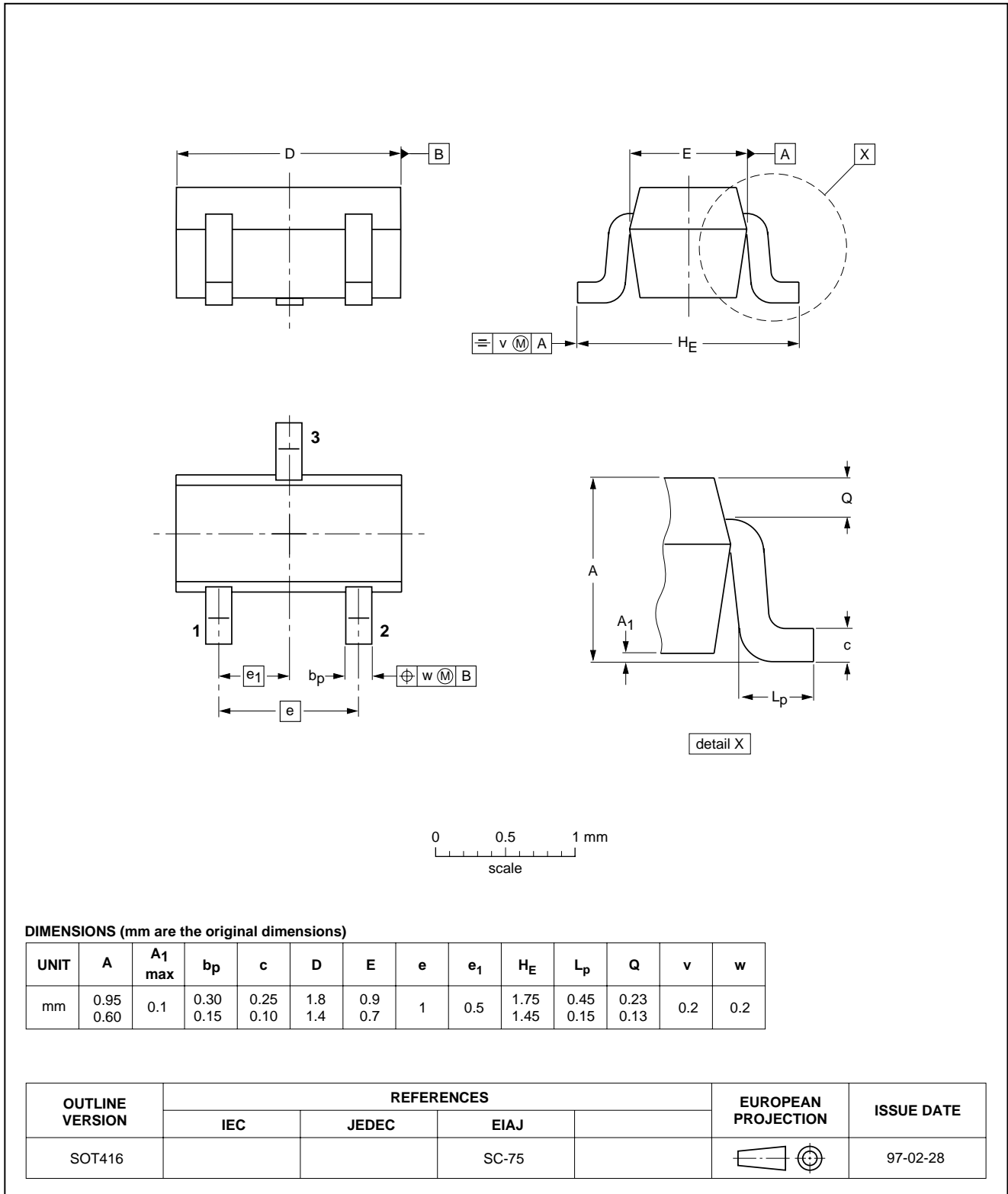
PNP resistor-equipped transistors;  
R1 = 22 kΩ, R2 = 22 kΩ

PDTA124E series

PACKAGE OUTLINES

Plastic surface mounted package; 3 leads

SOT416

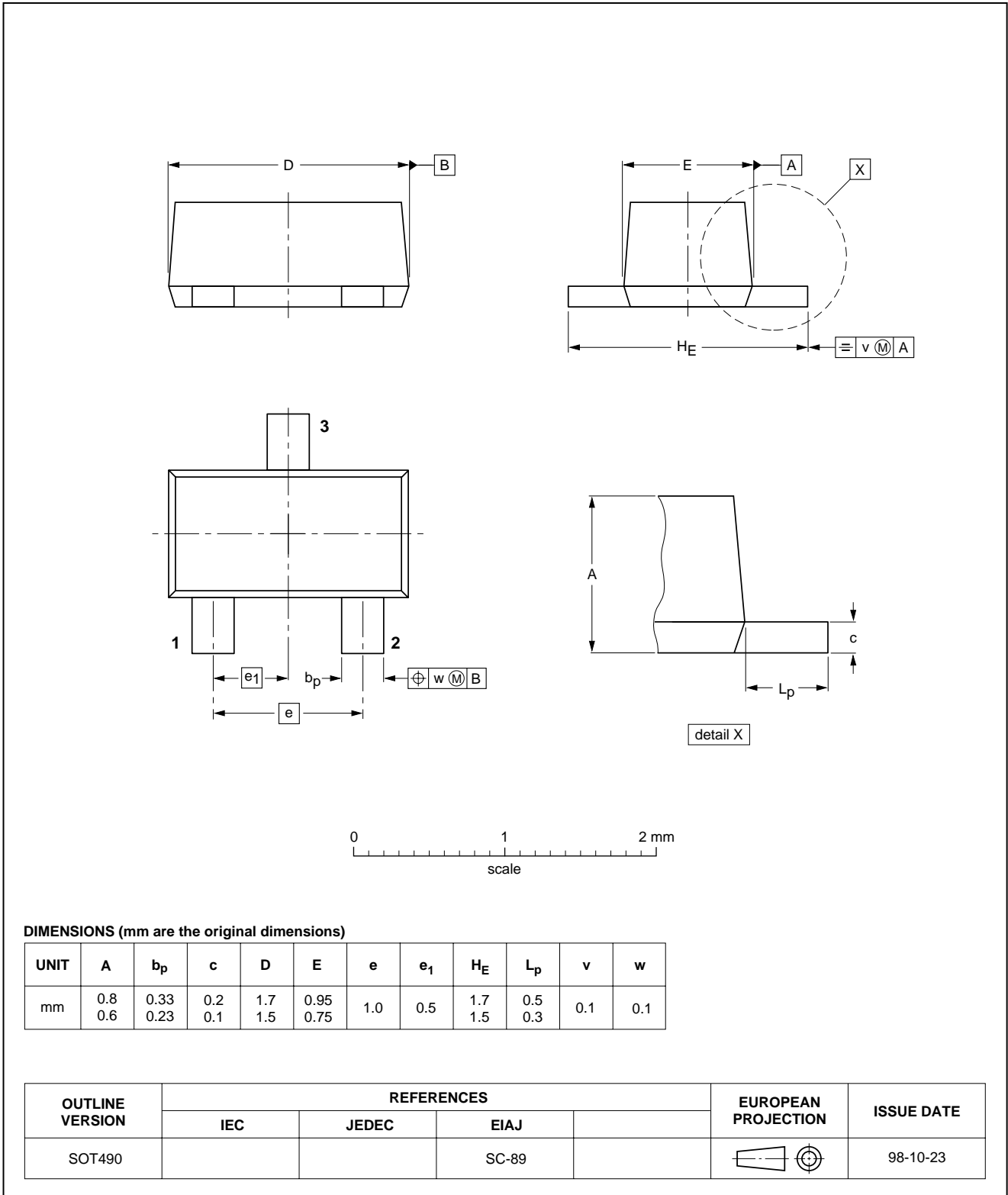


PNP resistor-equipped transistors;  
R1 = 22 kΩ, R2 = 22 kΩ

PDTA124E series

Plastic surface mounted package; 3 leads

SOT490

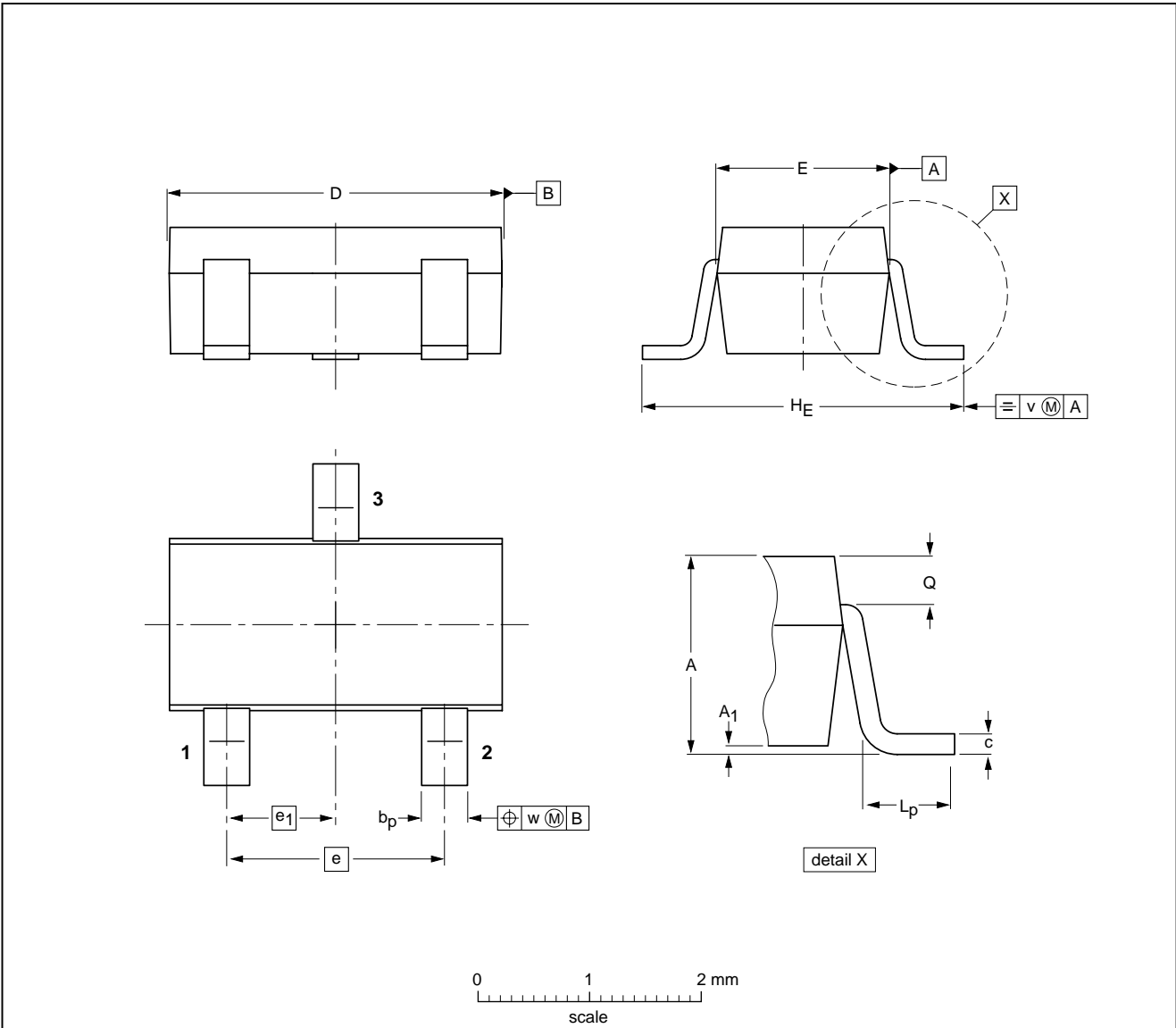


PNP resistor-equipped transistors;  
R1 = 22 kΩ, R2 = 22 kΩ

PDTA124E series

Plastic surface mounted package; 3 leads

SOT346



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w
mm	1.3 1.0	0.1 0.013	0.50 0.35	0.26 0.10	3.1 2.7	1.7 1.3	1.9	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT346		TO-236	SC-59			98-07-17

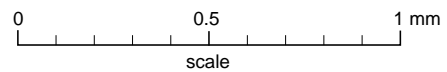
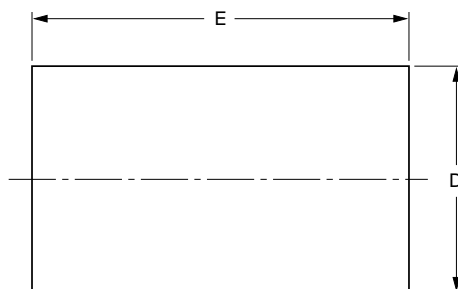
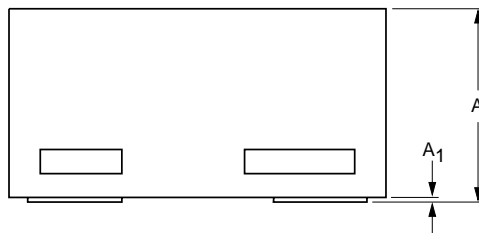
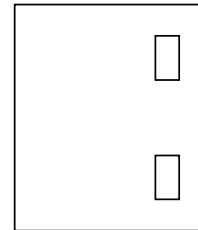
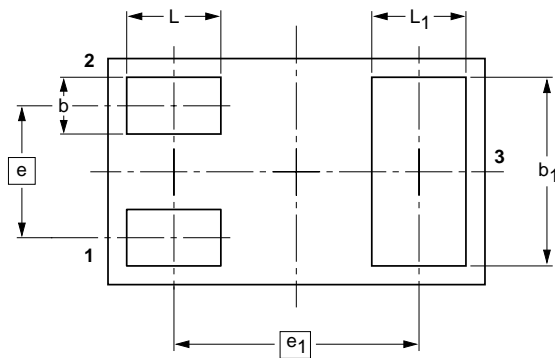


PNP resistor-equipped transistors;  
R1 = 22 kΩ, R2 = 22 kΩ

PDTA124E series

Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm

SOT883



DIMENSIONS (mm are the original dimensions)

UNIT	A <sup>(1)</sup>	A <sub>1</sub> max.	b	b <sub>1</sub>	D	E	e	e <sub>1</sub>	L	L <sub>1</sub>
mm	0.50 0.46	0.03	0.20 0.12	0.55 0.47	0.62 0.55	1.02 0.95	0.35	0.65	0.30 0.22	0.30 0.22

Note

1. Including plating thickness

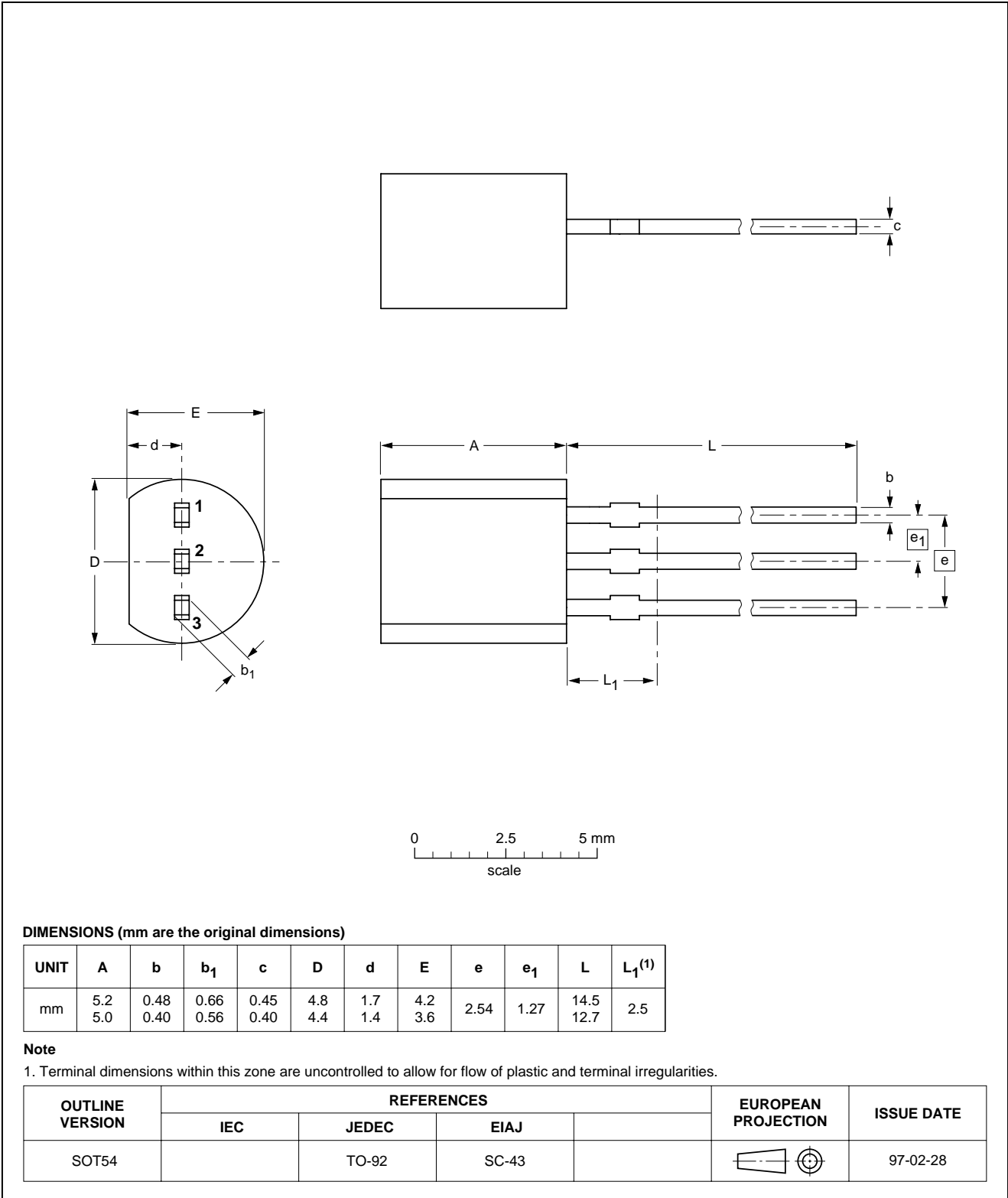
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT883			SC-101			03-02-05- 03-04-03

PNP resistor-equipped transistors;  
R1 = 22 kΩ, R2 = 22 kΩ

PDTA124E series

Plastic single-ended leaded (through hole) package; 3 leads

SOT54

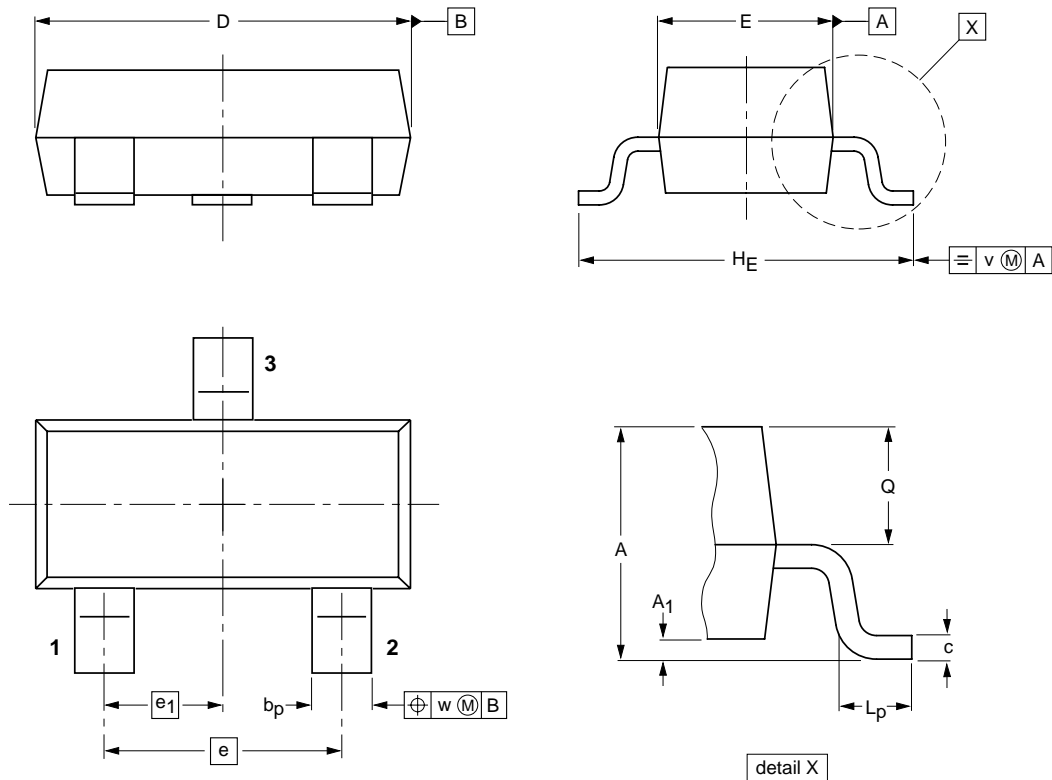


PNP resistor-equipped transistors;  
R1 = 22 kΩ, R2 = 22 kΩ

PDTA124E series

Plastic surface mounted package; 3 leads

SOT23



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max.	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

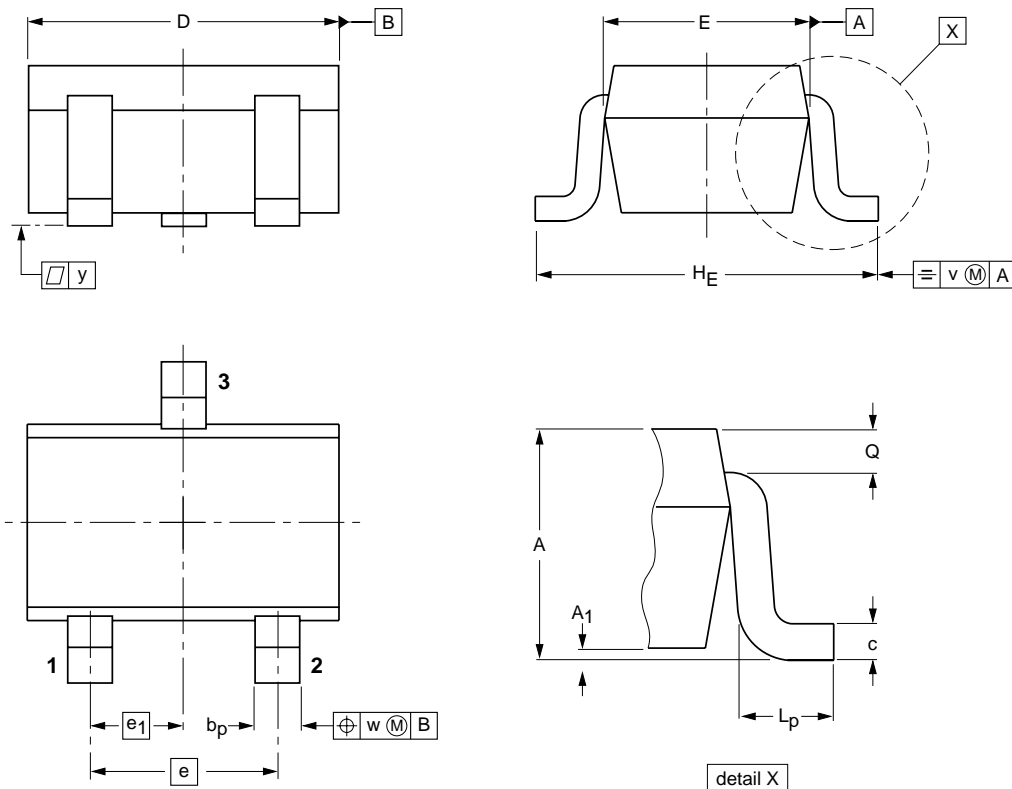
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23		TO-236AB				97-02-28- 99-09-13

PNP resistor-equipped transistors;  
R1 = 22 kΩ, R2 = 22 kΩ

PDTA124E series

Plastic surface mounted package; 3 leads

SOT323



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w
mm	1.1 0.8	0.1	0.4 0.3	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT323			SC-70			97-02-28

PNP resistor-equipped transistors;  
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PDTA124E series

#### DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**NOTES**

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PDTA124E series

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**NOTES**

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