

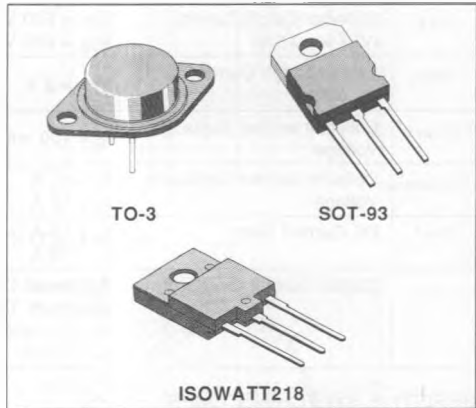
HIGH VOLTAGE, HIGH POWER, FAST SWITCHING

DESCRIPTION

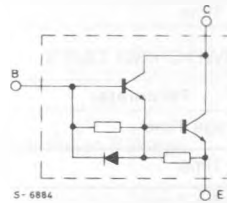
The SGSD00030, SGSD00031 and SGSD00031FI are silicon multi-epitaxial planar NPN transistors in monolithic Darlington configuration with integrated speed-up diode, mounted respectively in the TO-3 metal case, TO-218 plastic package and ISOWATT218 fully isolated package.

It has a parasitic collector-emitter diode, so that an external fast recovery free wheeling can be added.

They are particularly suitable as output stage in high power, fast switching applications.



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value			Unit
V_{CER}	Collector-emitter Voltage ($R_{BE} = 50\Omega$)	650			V
V_{CEO}	Collector-emitter Voltage ($I_B = 0$)	400			V
I_C	Collector-current	28			A
I_{CM}	Collector Peak Current ($t_p < 10ms$)	40			A
I_B	Base Current	6			A
I_{BM}	Base Peak Current ($t_p < 10 ms$)	12			A
		TO-3	TO-218	ISOWATT218	
P_{Tot}	Total Power Dissipation at $T_c < 25^\circ C$	150	125	60	W
T_{stg}	Storage Temperature	- 65 to 175	- 65 to 150	- 65 to 150	$^\circ C$
T_j	Max. Operating Junction Temperature	175	150	150	$^\circ C$

THERMAL DATA

			TO-3	TO-218	ISOWATT218	
$R_{th(j-case)}$	Thermal Resistance Junction-case	Max	1	1	2.08	°C/W

ELECTRICAL CHARACTERISTICS ($T_{case} = 25\text{ °C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CEV}	Collector Cutoff Current ($V_{BE} = -15\text{ V}$)	$V_{CE} = 600\text{ V}$ $V_{CE} = 600\text{ V}$ $T_{case} = 100\text{ °C}$			100 2	μA mA
I_{EBO}	Emitter Cutoff Current ($I_C = 0$)	$V_{EB} = 2\text{ V}$			30	mA
$V_{CE0(sus)}^*$	Collector-emitter Sustaining Voltage	$I_C = 100\text{ mA}$	400			V
$V_{CE(sat)}^*$	Collector-emitter Saturation Voltage	$I_C = 10\text{ A}$ $I_B = 0.1\text{ A}$ $I_C = 18\text{ A}$ $I_B = 1.8\text{ A}$			2.5 3.5	V V
h_{FE}^*	DC Current Gain	$I_C = 10\text{ A}$ $V_{CE} = 5\text{ V}$ $I_C = 18\text{ A}$ $V_{CE} = 5\text{ V}$	30 20			
I_{ol}	Output Current Overload	Accidental Overload Switch-off Current $V_{clamp} = 400\text{ V}$ $L = 100\text{ }\mu\text{H}$ $t_{ol} = 10\text{ }\mu\text{s}$ $T_j = 125\text{ °C}$	28			A

RESISTIVE SWITCHING TIMES

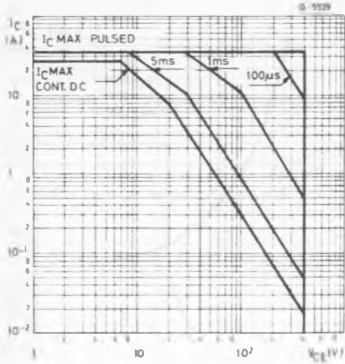
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
t_s	Turn-on Time	$V_{CC} = 250\text{ V}$ $I_C = 12\text{ A}$ $I_{B1} = 0.1\text{ A}$ $V_{BE(off)} = -5\text{ V}$			0.6	μs
t_s	Storage Time				1.5	μs
t_f	Fall Time				0.6	μs

INDUCTIVE SWITCHING TIMES

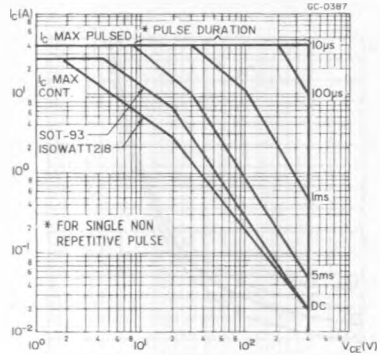
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
t_s	Storage Time	$V_{clamp} = 250\text{ V}$ $I_C = 12\text{ A}$ $I_{B1} = 0.1\text{ A}$ $V_{BE(off)} = -5\text{ V}$ $L = 180\text{ }\mu\text{H}$			1.5	μs
t_f	Fall Time				0.5	μs
t_s	Storage Time	$V_{clamp} = 250\text{ V}$ $I_C = 18\text{ A}$ $I_{B1} = 1.8\text{ A}$ $V_{BE(off)} = -5\text{ V}$ $L = 180\text{ }\mu\text{H}$			1.5	μs
t_f	Fall Time				0.7	μs

* Pulsed : pulse duration = 300 μs , duty cycle = 1.5%.

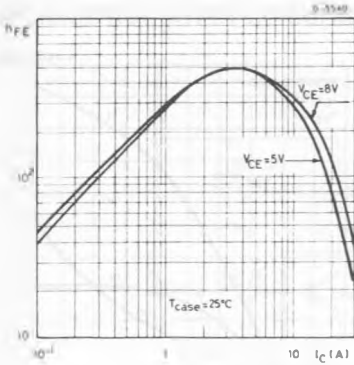
Safe Operating Areas (TO-3).



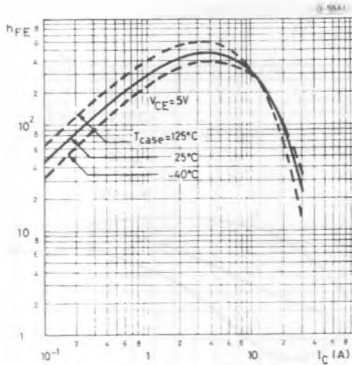
Safe Operating Areas (TO-218, ISOWATT218).



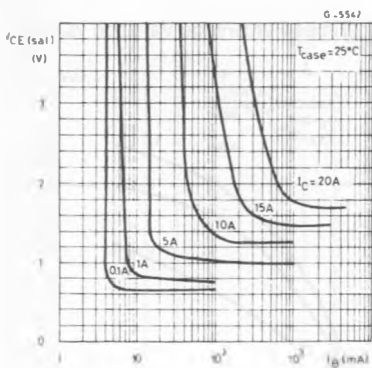
DC Current Gain.



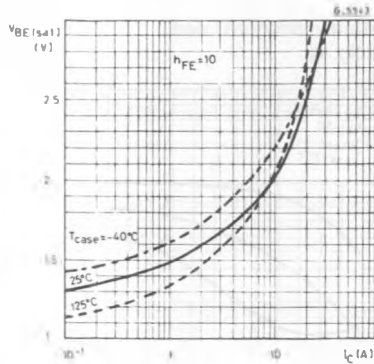
DC Current Gain.



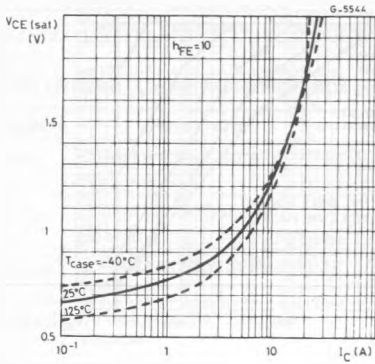
Collector-emitter Saturation Voltage.



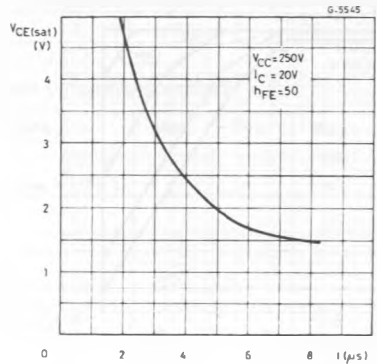
Base-emitter Saturation Voltage.



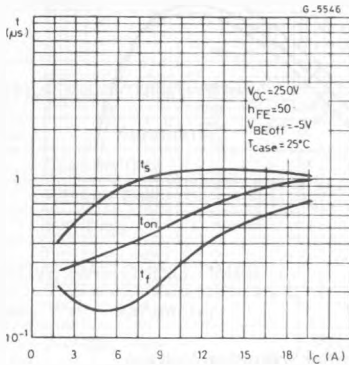
Collector-emitter Saturation Voltage.



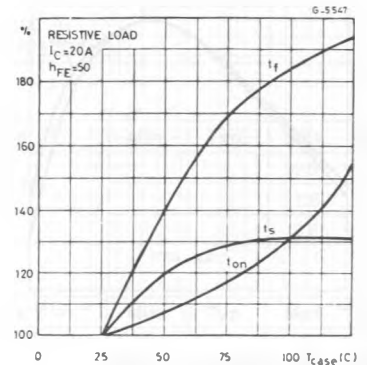
Collector-emitter Saturation Voltage Dynamic (test circuit fig. 2).



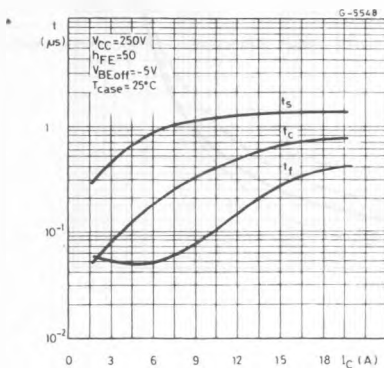
Switching Times Resistive Load (test circuit fig. 1).



Switching Times Percentage Variation vs. T_{case} .



Switching Times Inductive Load (test circuit fig. 1).



Switching Times Percentage Variation vs. T_{case} .

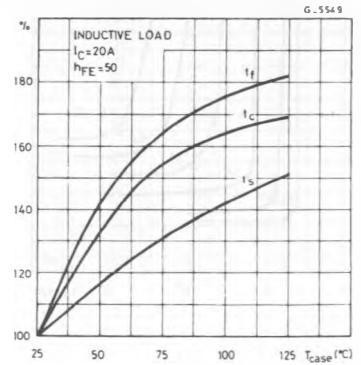
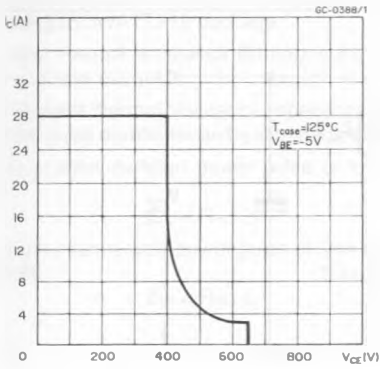
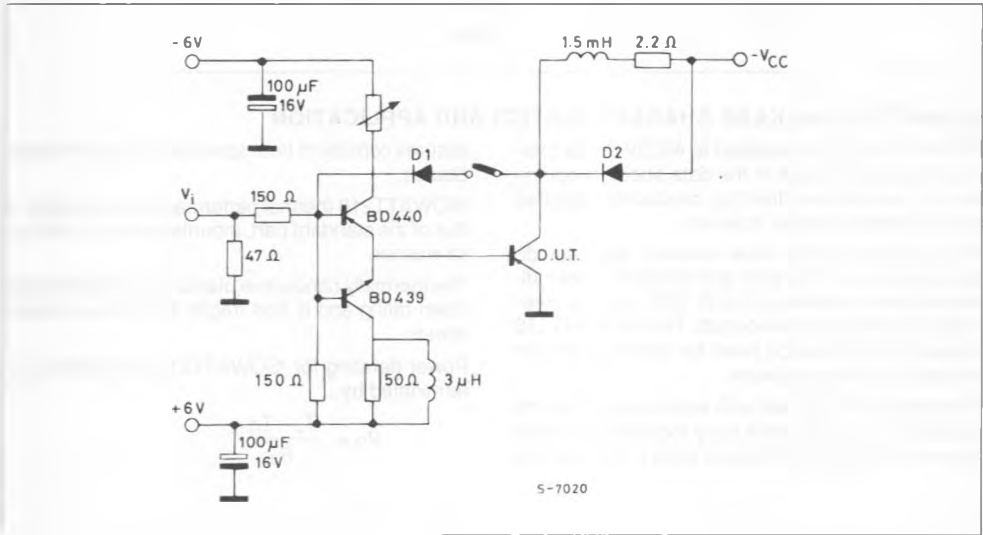


Figure 12 : Clamped Reverse Bias Safe Operating Area.



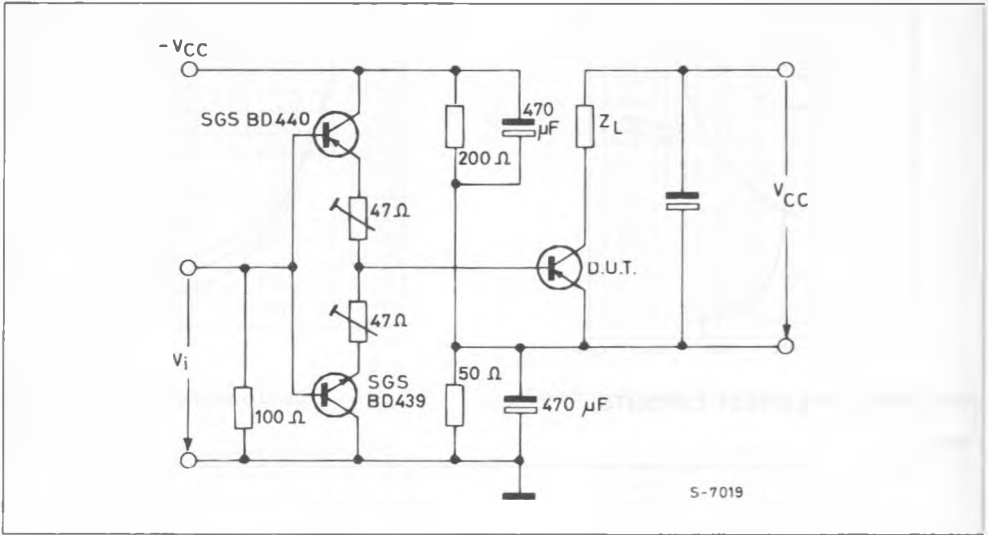
SWITCHING TIMES TEST CIRCUITS

Figure 1.



SWITCHING TIMES TEST CIRCUITS (continued)

Figure 2.



ISOWATT218 PACKAGE CHARACTERISTICS AND APPLICATION

ISOWATT218 is fully isolated to 4000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.

The structure of the case ensures optimum distances between the pins and heatsink. These distances are in agreement with VDE and UL creepage and clearance standards. The ISOWATT218 package eliminates the need for external isolation so reducing fixing hardware.

The package is supplied with leads longer than the standard TO-218 to allow easy mounting on pcbs. Accurate moulding techniques used in manufacture

assures consistent heat spreader-to-heatsink capacitance.

ISOWATT218 thermal performance is equivalent to that of the standard part, mounted with a 0.1mm mica washer.

The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets.

Power derating for ISOWATT218 packages is determined by :

$$P_D = \frac{T_J - T_C}{R_{th}}$$

HERMAL IMPEDANCE OF ISOWATT218 PACKAGE

Figure 2 illustrates the elements contributing to the thermal resistance of a transistor heatsink assembly using ISOWATT218 package.

The total thermal resistance $R_{th}(tot)$ is the sum of each of these elements.

The transient thermal resistance impedance, Z_{th} for different pulse durations can be estimated as follows :

1. For a short duration power pulse of less than 1ms :

$$Z_{th} < R_{thJ-C}$$

2. For an intermediate power pulse of 5ms to 50ms seconds :

$$Z_{th} = R_{thJ-C}$$

3. For long power pulses of the order of 500ms seconds or greater :

$$Z_{th} = R_{thJ-C} + R_{thC-HS} + R_{thHS-amb}$$

It is often possible to discern these areas on transient thermal impedance curves.

Figure 2.

