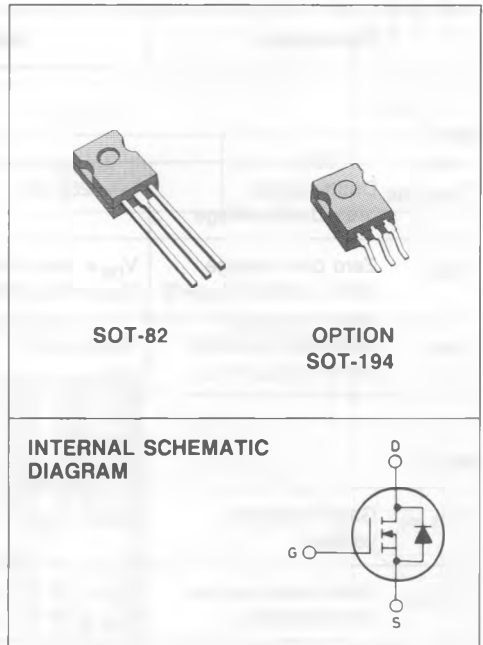


## N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
SGSP239	500 V	8.5 Ω	1.2 A

- HIGH SPEED SWITCHING APPLICATIONS
  - ULTRA FAST SWITCHING
  - EASY DRIVE FOR REDUCED COST AND SIZE
- INDUSTRIAL APPLICATIONS:**
- SWITCHING MODE POWER SUPPLIES

N-channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. These include switching power supplies, solenoid drivers and drive circuits for power bipolar transistors.



### ABSOLUTE MAXIMUM RATINGS

V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> = 0)	500	V
V <sub>DGR</sub>	Drain-gate voltage (R <sub>GS</sub> = 20 KΩ)	500	V
V <sub>GS</sub>	Gate-source voltage	±20	V
I <sub>D</sub>	Drain current (cont.) at T <sub>c</sub> = 25°C	1.2	A
I <sub>D</sub>	Drain current (cont.) at T <sub>c</sub> = 100°C	0.8	A
I <sub>DM</sub> (*)	Drain current (pulsed)	4.8	A
I <sub>OLM</sub> (*)	Drain inductive current, clamped	4.8	A
P <sub>tot</sub>	Total dissipation at T <sub>c</sub> < 25°C	40	W
	Derating factor	0.32	W/°C
T <sub>stg</sub>	Storage temperature	-65 to 150	°C
T <sub>j</sub>	Max. operating junction temperature	150	°C

(\*) Pulse width limited by safe operating area

## THERMAL DATA

$R_{thj \cdot case}$	Thermal resistance junction-case	max	3.12	$^{\circ}C/W$
$T_L$	Maximum lead temperature for soldering purpose		275	$^{\circ}C$

ELECTRICAL CHARACTERISTICS ( $T_{case} = 25^{\circ}C$  unless otherwise specified)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
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## OFF

$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu A$	$V_{GS} = 0$	500		V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$	$T_c = 125^{\circ}C$		250 1000	$\mu A$ $\mu A$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20 V$			$\pm 100$	nA

## ON (\*)

$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$	$I_D = 250 \mu A$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 V$ $V_{GS} = 10 V$	$I_D = 0.6 A$ $I_D = 0.6 A$			8.5 17	$\Omega$ $\Omega$

## DYNAMIC

$g_{fs}$	Forward transconductance	$V_{DS} = 25 V$	$I_D = 0.6 A$	0.65			mho
$C_{iss}$	Input capacitance	$V_{DS} = 25 V$	$f = 1 \text{ MHz}$		260	300	pF
$C_{oss}$	Output capacitance	$V_{GS} = 0$				80	pF
$C_{rss}$	Reverse transfer capacitance					40	pF

## SWITCHING

$t_{d(on)}$	Turn-on time	$V_{DD} = 250 V$	$I_D = 0.6 A$		15	20	ns
$t_r$	Rise time	$V_i = 10 V$	$R_i = 4.7 \Omega$		15	30	ns
$t_{d(off)}$	Turn-off time	(see test circuit)			30	60	ns
$t_f$	Fall time				20	45	ns

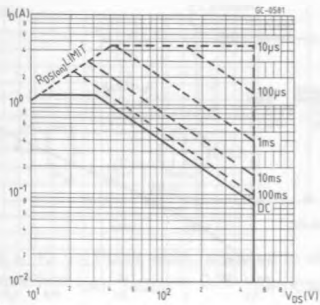
ELECTRICAL CHARACTERISTICS (Continued)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current			1.2	A
$I_{SDM}^*$	Source-drain current (pulsed)			4.8	A
$V_{SD}$	Forward on voltage	$I_{SD} = 1.2 \text{ A}$	$V_{GS} = 0$	1.15	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 1.2 \text{ A}$ $di/dt = 25 \text{ A}/\mu\text{s}$	$V_{GS} = 0$	350	ns

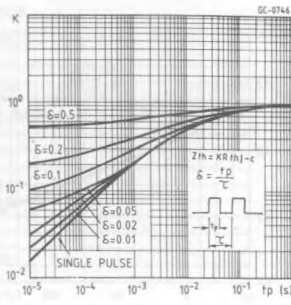
(\*) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

(\*) Pulse width limited by safe operating area

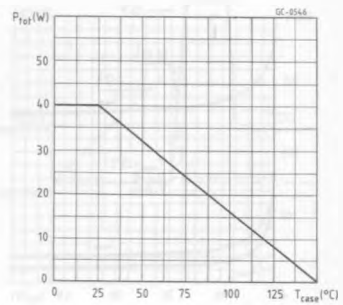
Safe operating areas



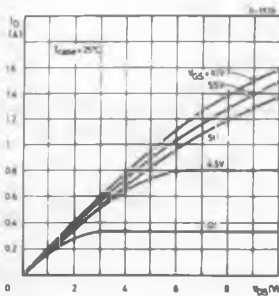
Thermal impedance



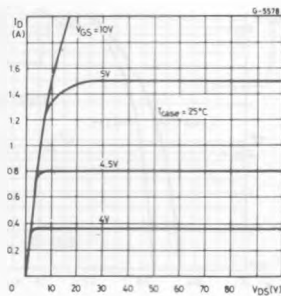
Derating curve



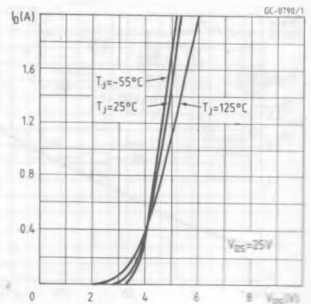
Output characteristics



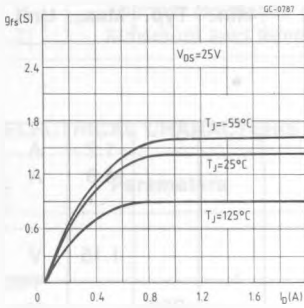
Output characteristics



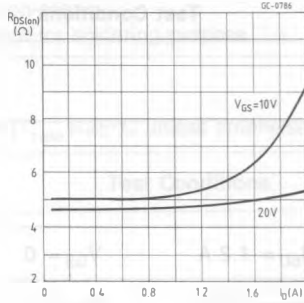
Transfer characteristics



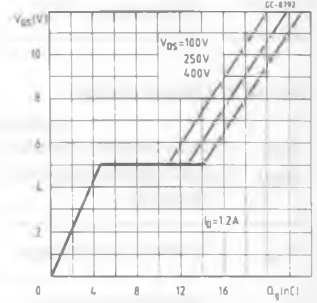
Transconductance



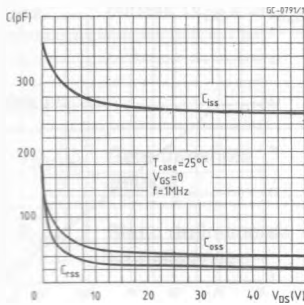
Static drain-source on resistance



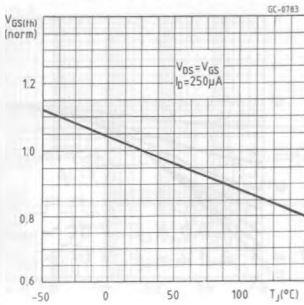
Gate charge vs gate-source voltage



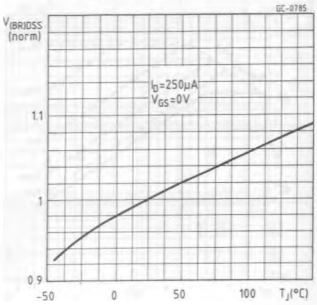
Capacitance variation



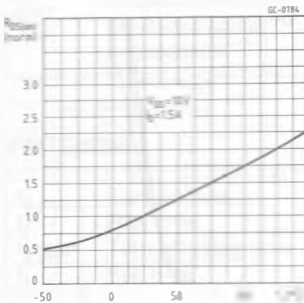
Normalized gate threshold voltage vs temperature



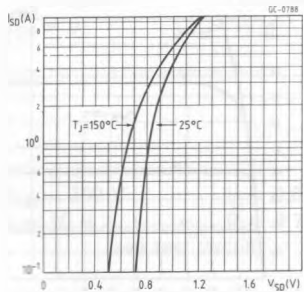
Normalized breakdown voltage vs temperature



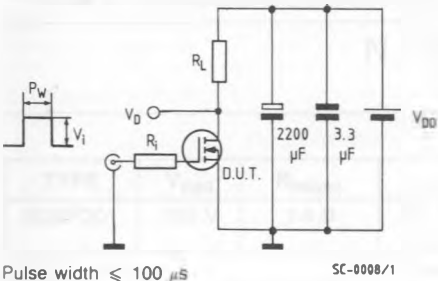
Normalized on resistance vs temperature



Source-drain diode forward characteristics

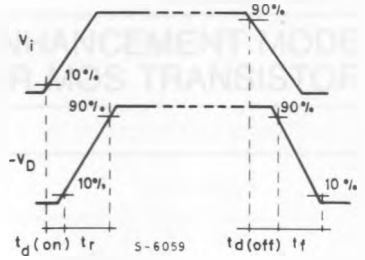


Switching times test circuit for resistive load

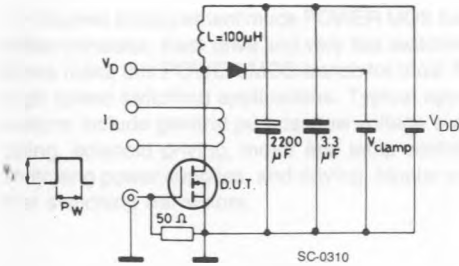


Pulse width  $\leq 100 \mu\text{s}$   
 Duty cycle  $\leq 2\%$

Switching time waveforms for resistive load

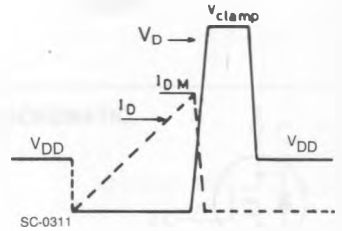


Clamped inductive load test circuit

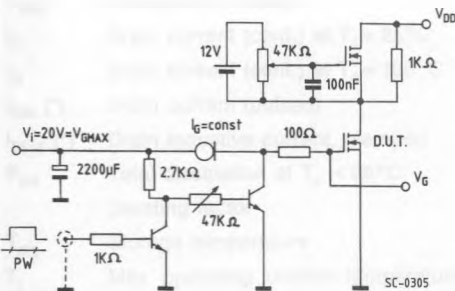


$V_i = 12 \text{ V}$  - Pulse width: adjusted to obtain specified  $I_{DM}$ .  $V_{clamp} = 0.75 V_{(BR)}$  DSS.

Clamped inductive waveforms



Gate charge test circuit



PW adjusted to obtain required  $V_G$

Body-drain diode  $t_{rr}$  measurement  
 Jedec test circuit

