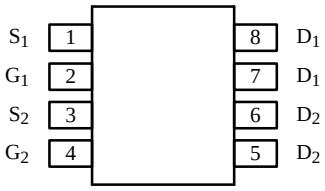
Dual Enhancement-Mode MOSFET (N- and P-Channel)

Product Summary

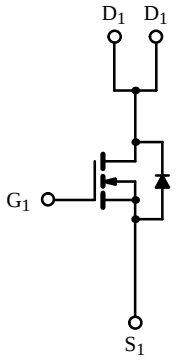
	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	60	0.055 @ V_{GS} = 10 V	± 4.5
		0.075 @ V_{GS} = 4.5 V	± 3.9
P-Channel	–30	0.053 @ V_{GS} = –10 V	± 5.1
		0.095 @ V_{GS} = –4.5 V	± 3.8

175° C Rated
Maximum Junction Temperature
TrenchFET™
Power MOSFETs

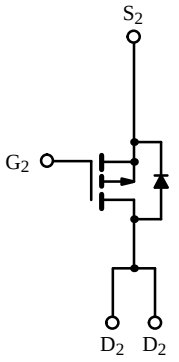
SO-8



Top View



N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	60	–30	V
Gate-Source Voltage		V_{GS}	± 20	± 20	
Continuous Drain Current (T_J = 175°C)[a]	T_A = 25°C	I_D	± 4.5	± 5.1	A
	T_A = 70°C		± 3.8	± 4.3	
Pulsed Drain Current		I_{DM}	± 20	± 20	
Continuous Source Current (Diode Conduction)[a]		I_S	2.0	–2.0	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.4		W
	T_A = 70°C		1.7		
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 175		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P- Channel	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	62.5	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1240. A SPICE Model data sheet is available for this product (FaxBack document #5153).

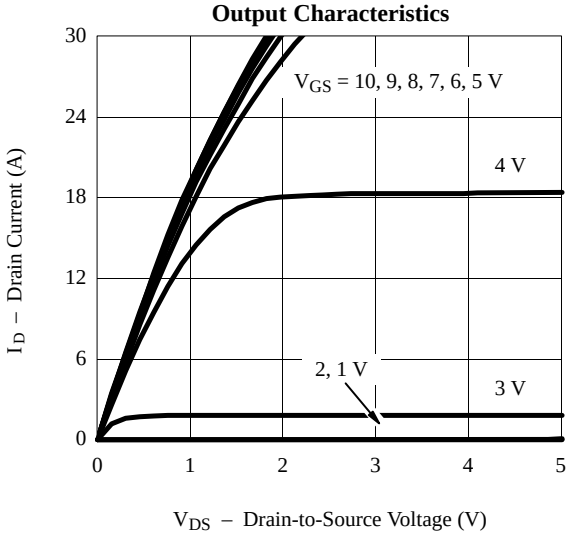
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition		Min	Typ[a]	Max	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1			V
		V_{DS} = V_{GS}, I_D = –250 µA	P-Ch	–1			
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V	N-Ch			± 100	nA
			P-Ch			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V	N-Ch			2	µA
		V_{DS} = –30 V, V_{GS} = 0 V	P-Ch			–2	
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55°C	N-Ch			25	
		V_{DS} = –30 V, V_{GS} = 0 V, T_J = 55°C	P-Ch			–25	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	N-Ch	20			A
		V_{DS} ≤ –5 V, V_{GS} = –10 V	P-Ch	–20			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 4.5 A	N-Ch		0.045	0.055	Ω
		V_{GS} = –10 V, I_D = –5.1 A	P-Ch		0.043	0.053	
		V_{GS} = 4.5 V, I_D = 3.9 A	N-Ch		0.055	0.075	
		V_{GS} = –4.5 V, I_D = –3.8 A	P-Ch		0.070	0.095	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 4.5 A	N-Ch		13		S
		V_{DS} = –15 V, I_D = –5.1 A	P-Ch		11		
Diode Forward Voltage[b]	V_{SD}	I_S = 2.0 A, V_{GS} = 0 V	N-Ch		0.9	1.2	V
		I_S = –2.0 A, V_{GS} = 0 V	P-Ch		0.8	–1.2	
Dynamic[a]							
Total Gate Charge	Q_g	N-Channel V_{DS} = 30 V, V_{GS} = 10 V, I_D = 4.5 A P-Channel V_{DS} = –15 V, V_{GS} = –10 V I_D = –5.1A	N-Ch		19	30	nC
			P-Ch		16	25	
Gate-Source Charge	Q_{gs}		N-Ch		4		
			P-Ch		5		
Gate-Drain Charge	Q_{gd}		N-Ch		3		
			P-Ch		2		
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 30 V, R_L = 30 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω P-Channel V_{DD} = –15 V, R_L = 15 Ω I_D ≅ –1 A, V_{GEN} = –10 V, R_G = 6 Ω	N-Ch		13	20	ns
			P-Ch		9	15	
Rise Time	t_r		N-Ch		11	20	
			P-Ch		13	20	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		36	60	
			P-Ch		25	40	
Fall Time	t_f		N-Ch		11	20	
			P-Ch		15	25	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2 A, di/dt = 100 A/µs	N-Ch		35	60	
		I_F = –2 A, di/dt = 100 A/µs	P-Ch		60	90	

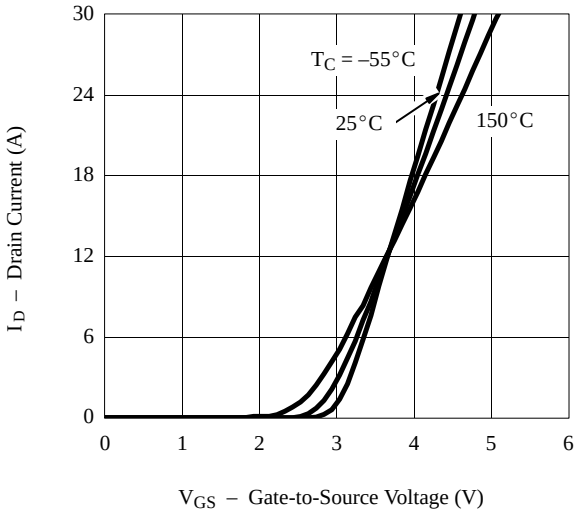
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25°C Unless Otherwise Noted) N-Channel

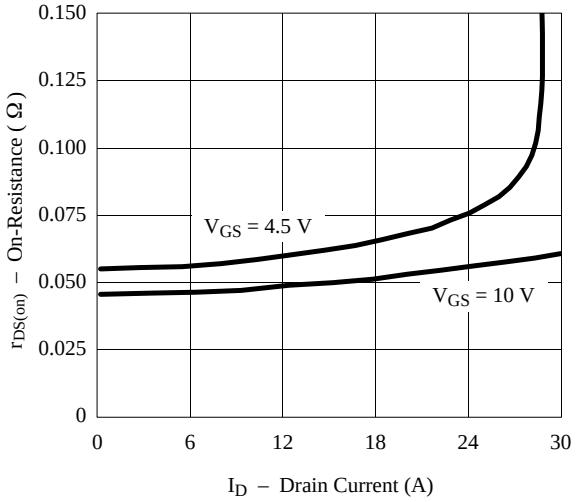
Output Characteristics



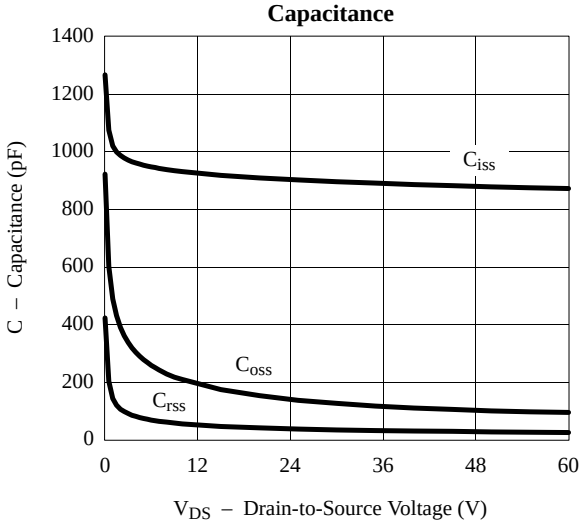
Transfer Characteristics



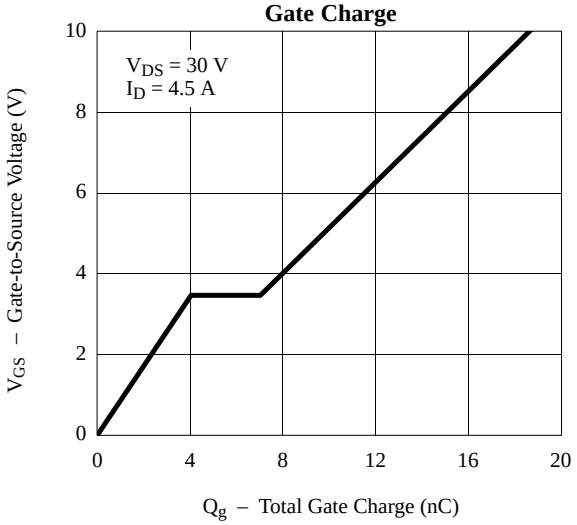
On-Resistance vs. Drain Current



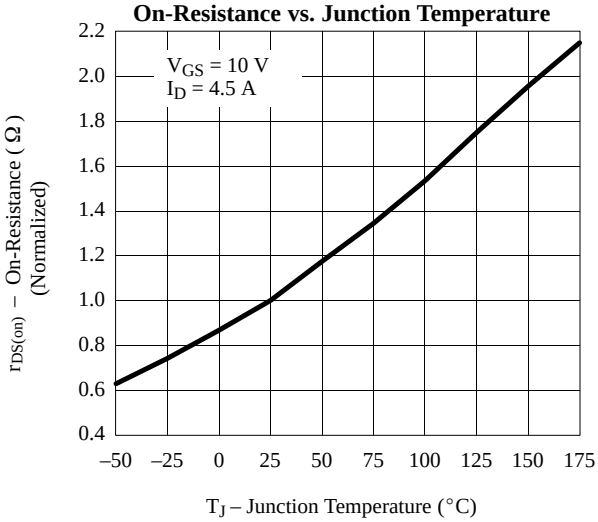
Capacitance



Gate Charge

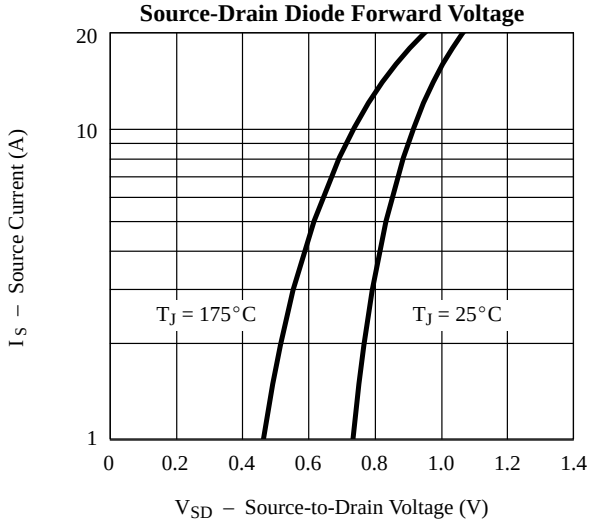


On-Resistance vs. Junction Temperature

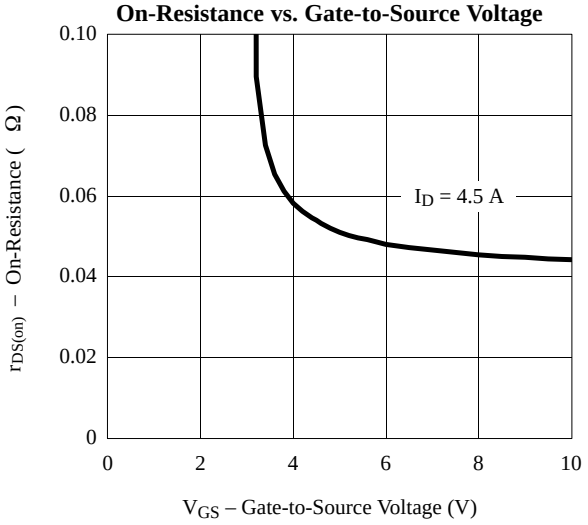


Typical Characteristics (25°C Unless Otherwise Noted) N-Channel

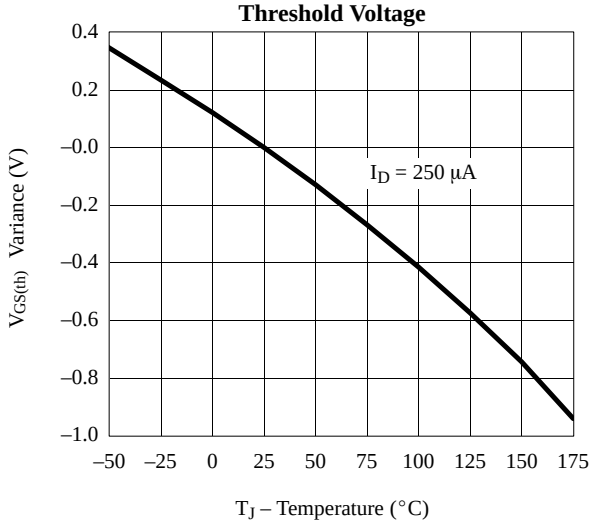
Source-Drain Diode Forward Voltage



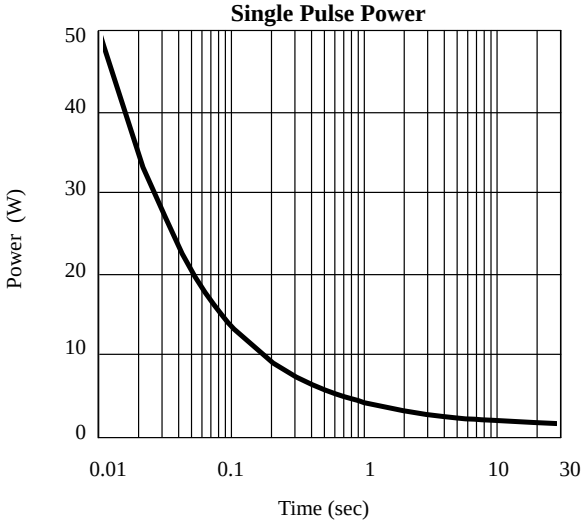
On-Resistance vs. Gate-to-Source Voltage



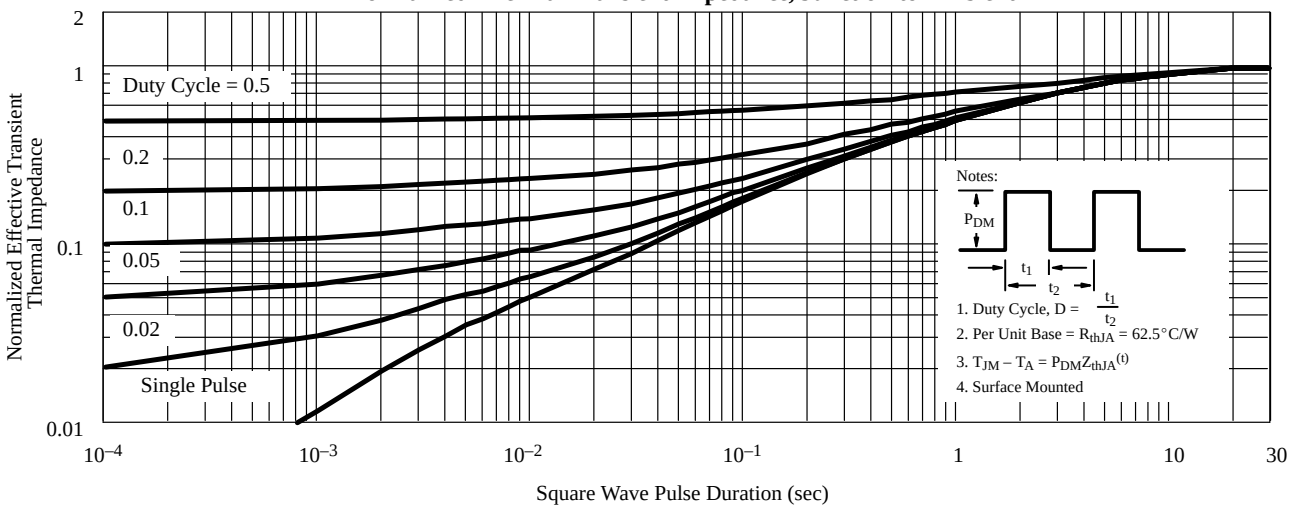
Threshold Voltage



Single Pulse Power

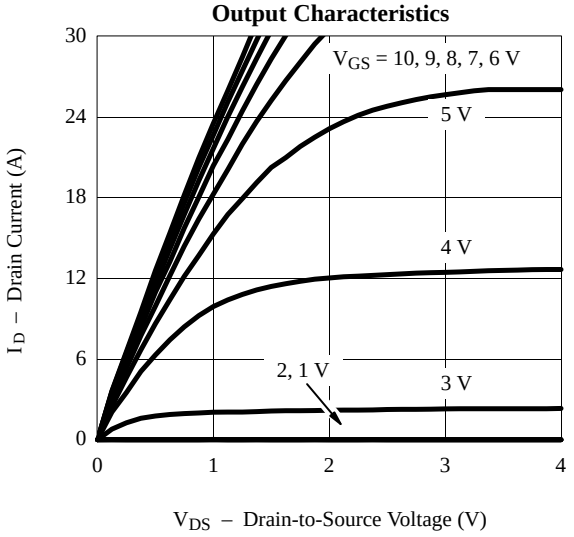


Normalized Thermal Transient Impedance, Junction-to-Ambient

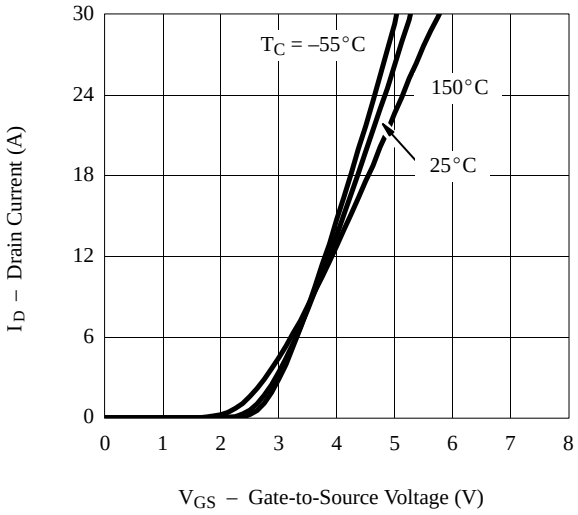


Typical Characteristics (25°C Unless Otherwise Noted) P-Channel

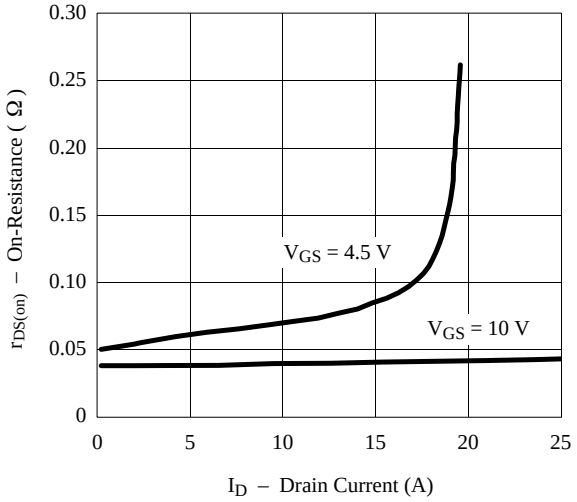
Output Characteristics



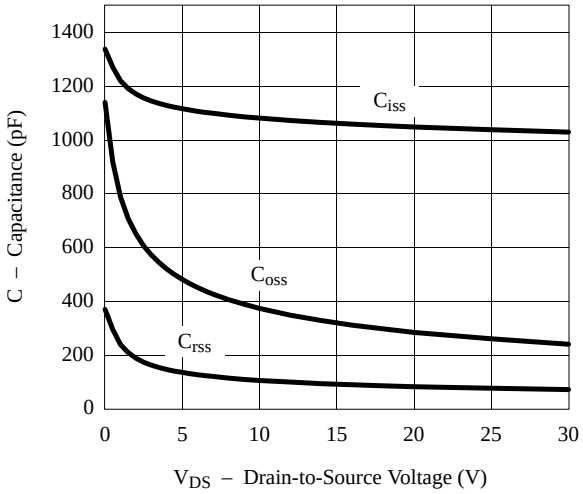
Transfer Characteristics



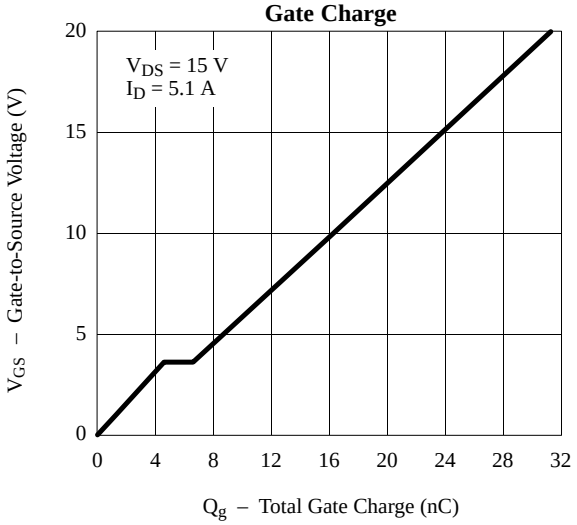
On-Resistance vs. Drain Current



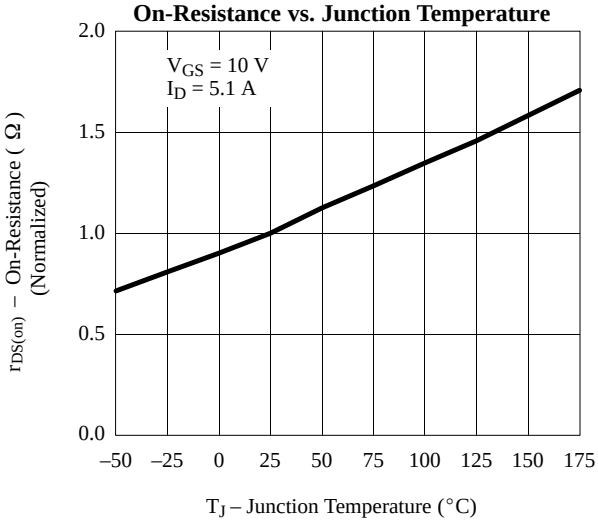
Capacitance



Gate Charge

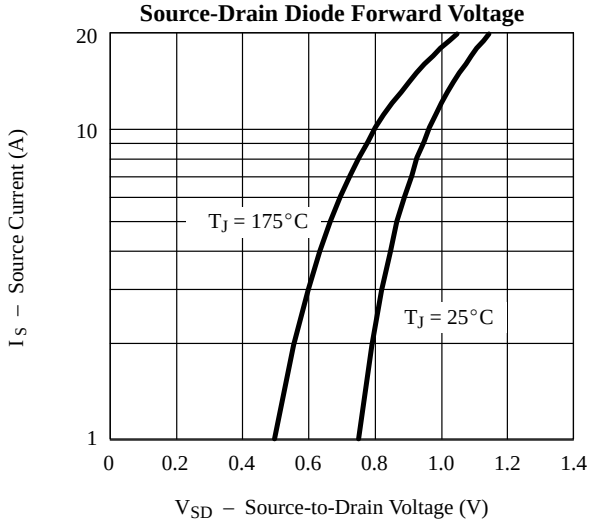


On-Resistance vs. Junction Temperature

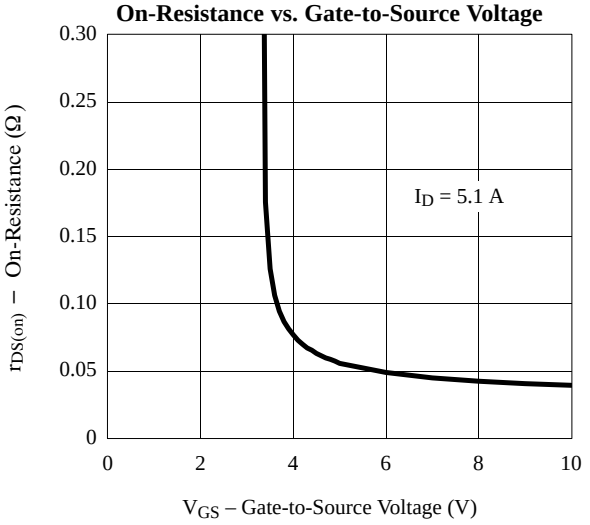


Typical Characteristics (25°C Unless Otherwise Noted) P-Channel

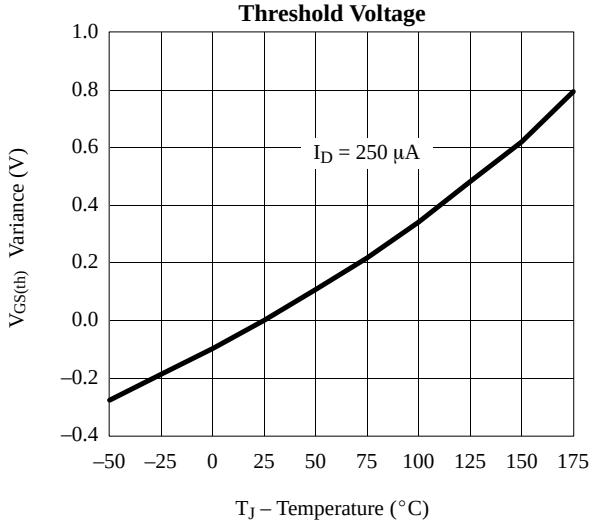
Source-Drain Diode Forward Voltage



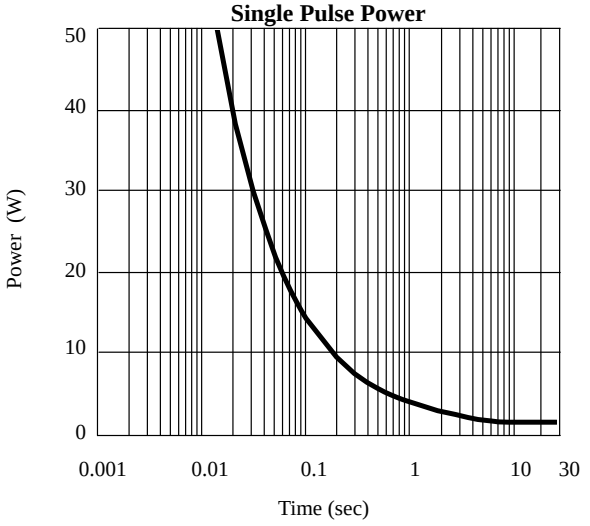
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient