



N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.025 @ $V_{GS} = 10$ V	9.3
	0.028 @ $V_{GS} = 6.0$ V	8.8

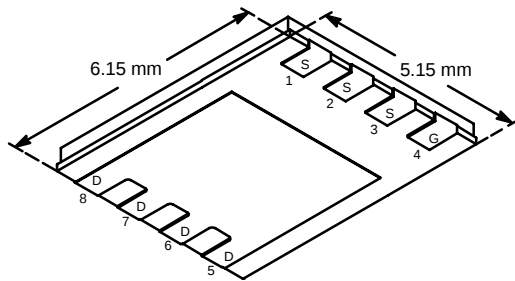
FEATURES

- TrenchFET® Power MOSFETS
- New Low Thermal Resistance PowerPAK™ Package with Low 1.07-mm Profile
- PWM Optimized for Fast Switching

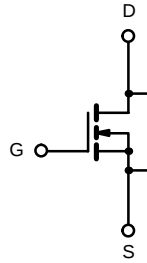
APPLICATIONS

- Primary Side Switch for High Density DC/DC
- Telecom/Server 48-V, Full-/Half-Bridge DC/DC
- Industrial and 42-V Automotive

PowerPAK™ SO-8



Bottom View



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V _{DS}	100		V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	9.3	5.7	A
	T _A = 85°C		6.7	4.1	
Pulsed Drain Current		I _{DM}	40		
Avalanche Current	L = 0.1 mH	I _{AS}	30		
Single Avalanche Energy (Duty Cycle ≤ 1%)		E _{AS}	45		mJ
Continuous Source Current (Diode Conduction) ^a		I _S	4.3	1.6	A
Maximum Power Dissipation ^a	T _A = 25°C	P _D	5.2	1.9	W
	T _A = 85°C		2.7	1.0	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	R_{thJA}	19	24	$^\circ\text{C/W}$
	Steady State		52	65	
Maximum Junction-to-Case	Steady State	R_{thJC}	1.5	1.8	

Notes

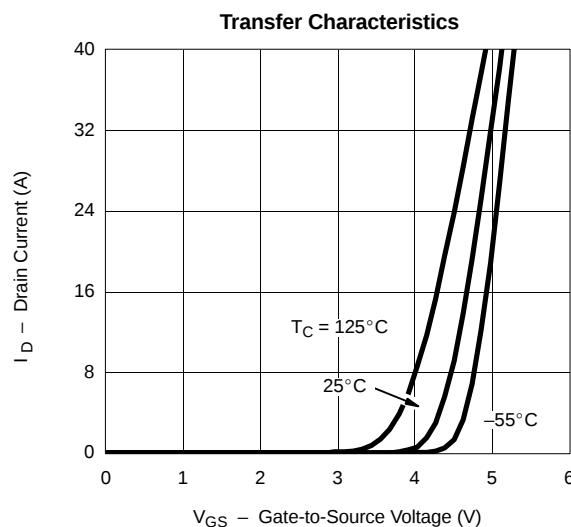
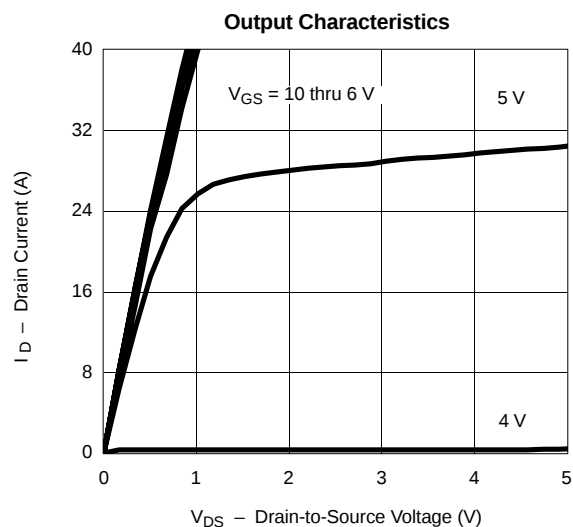
a. Surface Mounted on 1" x 1" FR4 Board.

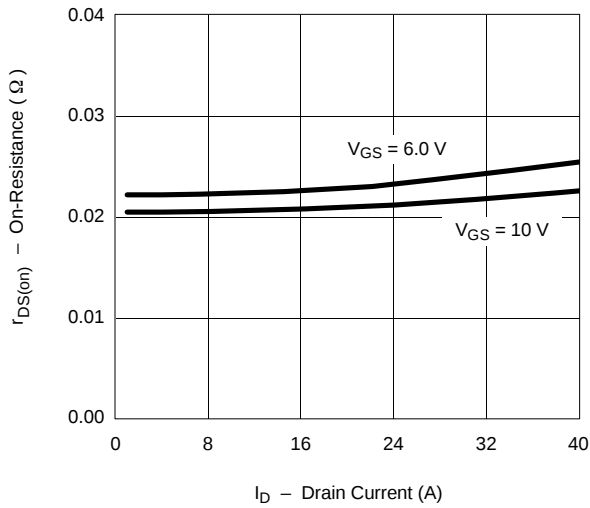
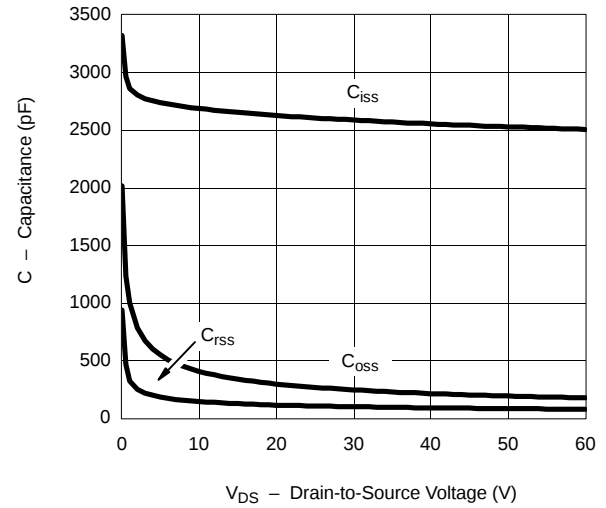
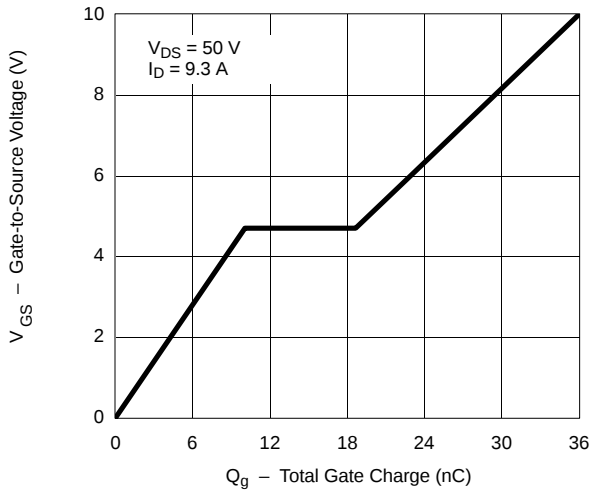
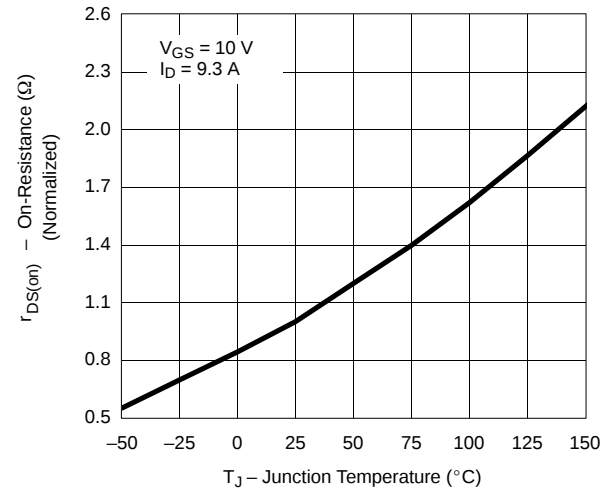
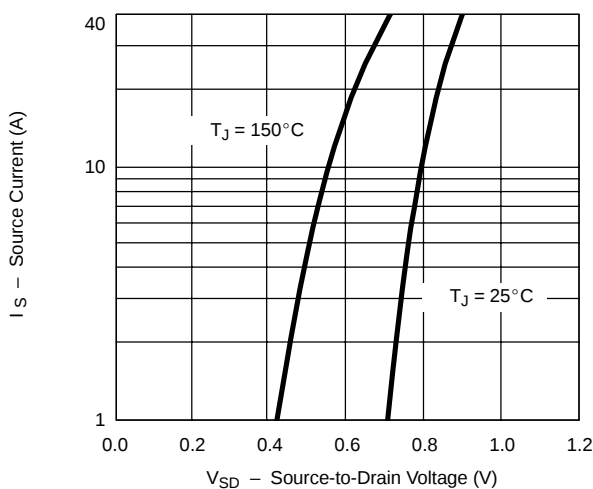
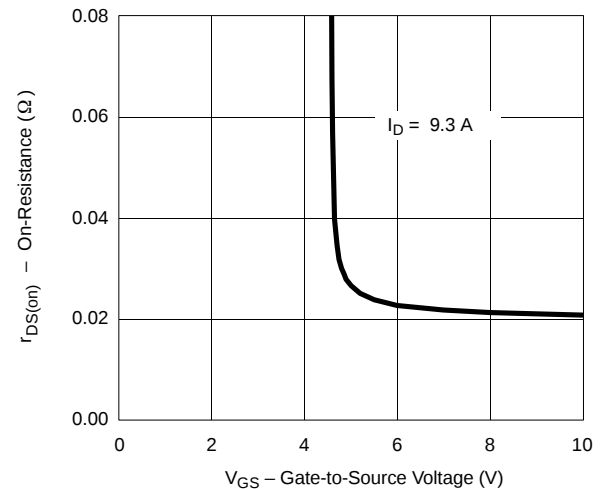
SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	2			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 80\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 85^\circ\text{C}$			20	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$, $V_{GS} = 10\ \text{V}$	40			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 9.3\ \text{A}$		0.021	0.025	Ω
		$V_{GS} = 6.0\ \text{V}$, $I_D = 8.8\ \text{A}$		0.023	0.028	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}$, $I_D = 9.3\ \text{A}$		35		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 4.3\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 50\ \text{V}$, $V_{GS} = 10\ \text{V}$, $I_D = 9.3\ \text{A}$		36	44	nC
Gate-Source Charge	Q_{gs}			10		
Gate-Drain Charge	Q_{gd}			8.6		
Gate Resistance	R_g			1.27		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\ \text{V}$, $R_L = 50\ \Omega$ $I_D \cong 1\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_G = 6\ \Omega$		20	40	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			46	90	
Fall Time	t_f			26	50	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 4.3\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		50	80	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)****On-Resistance vs. Drain Current****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature****Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage**

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

