

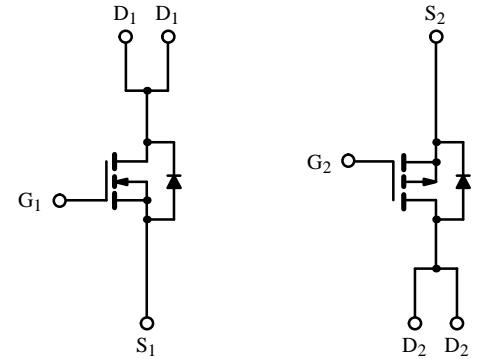
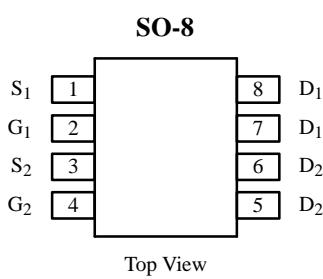
Dual Enhancement-Mode MOSFET (N- and P-Channel)

Product Summary

	V _{DS} (V)	r _{D(on)} (Ω)	I _D (A)
N-Channel	20	0.05 @ V _{GS} = 4.5 V	± 5.0
		0.06 @ V _{GS} = 3.0 V	± 4.2
		0.08 @ V _{GS} = 2.7 V	± 3.6
P-Channel	-20	0.11 @ V _{GS} = -4.5 V	± 3.4
		0.15 @ V _{GS} = -3.0 V	± 2.9
		0.19 @ V _{GS} = -2.7 V	± 2.6

Recommended upgrade: Si9529DY

Lower profile/smaller size—see LITE FOOT® equivalent: Si6552DQ



Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V _{DS}	20	-20	V
Gate-Source Voltage	V _{GS}	± 12	± 12	
Continuous Drain Current (T _J = 150°C) ^a	I _D	± 5.0	± 3.4	A
		± 4.0	± 2.8	
Pulsed Drain Current	I _{DM}	± 10	± 10	
Continuous Source Current (Diode Conduction) ^a	I _S	2.0	-2.0	
Maximum Power Dissipation ^a	P _D	2.0	2.0	W
		1.3	1.3	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	62.5	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1225.

Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

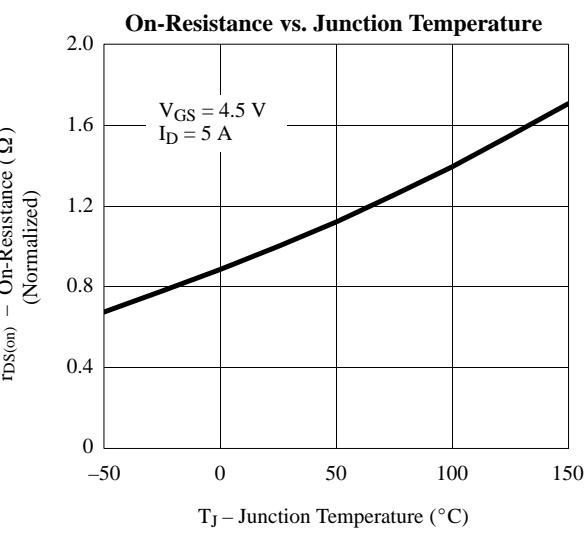
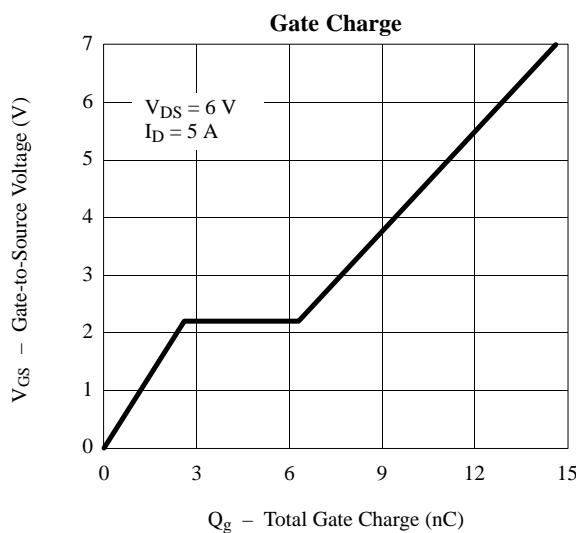
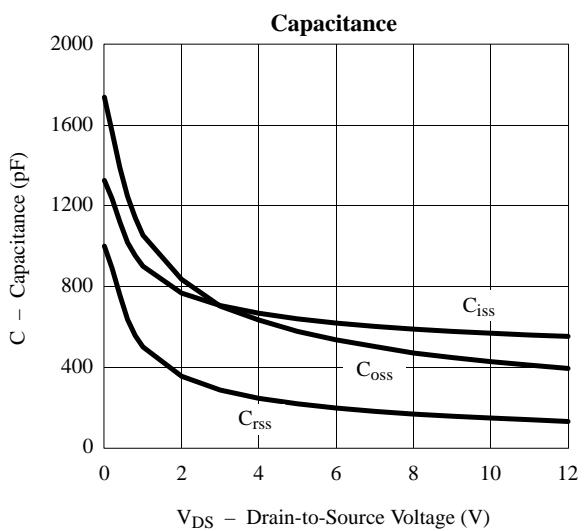
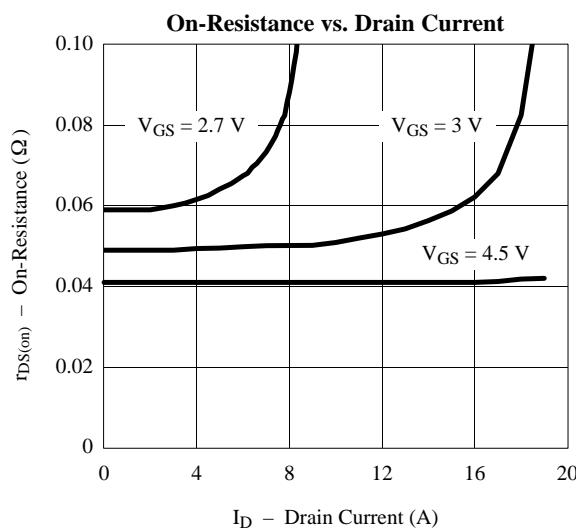
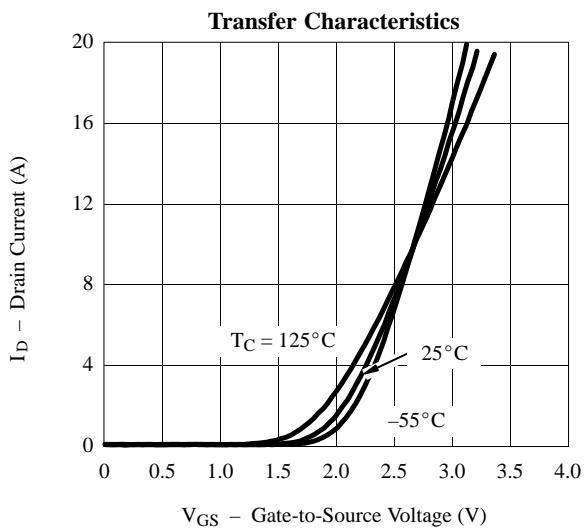
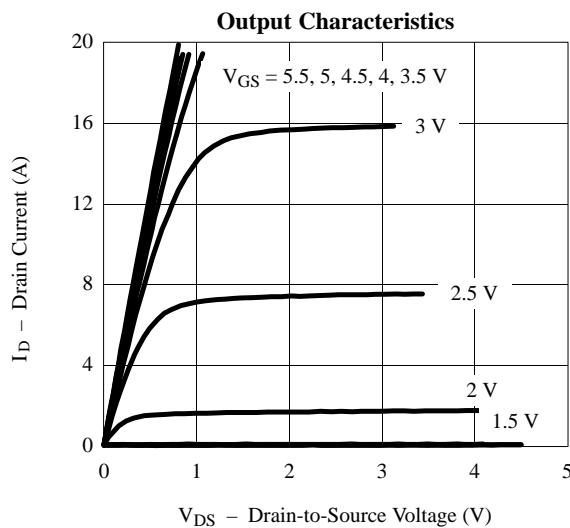
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	N-Ch	0.8	1.2	V
		$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	P-Ch	-0.8	-1.1	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$	N-Ch		± 100	nA
			P-Ch		± 100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}$	N-Ch		1	μA
		$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$	P-Ch		-1	
		$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 70^\circ\text{C}$	N-Ch		5	
		$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 70^\circ\text{C}$	P-Ch		-5	
On-State Drain Current ^b	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	N-Ch	10		A
		$V_{DS} \leq -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	P-Ch	-10		
Drain-Source On-State Resistance ^b	$r_{DS(\text{on})}$	$V_{GS} = 4.5 \text{ V}, I_D = 5.0 \text{ A}$	N-Ch	0.041	0.05	Ω
		$V_{GS} = -4.5 \text{ V}, I_D = -3.2 \text{ A}$	P-Ch	0.087	0.11	
		$V_{GS} = 3.0 \text{ V}, I_D = 3.9 \text{ A}$	N-Ch	0.052	0.06	
		$V_{GS} = -3.0 \text{ V}, I_D = -2.0 \text{ A}$	P-Ch	0.120	0.15	
		$V_{GS} = 2.7 \text{ V}, I_D = 1.0 \text{ A}$	N-Ch	0.060	0.08	
		$V_{GS} = -2.7 \text{ V}, I_D = -1.0 \text{ A}$	P-Ch	0.135	0.19	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 10 \text{ V}, I_D = 5.0 \text{ A}$	N-Ch	13		S
		$V_{DS} = -9 \text{ V}, I_D = -3.2 \text{ A}$	P-Ch	8		
Diode Forward Voltage ^b	V_{SD}	$I_S = 5.0 \text{ A}, V_{GS} = 0 \text{ V}$	N-Ch	0.9	1.2	V
		$I_S = -2.0 \text{ A}, V_{GS} = 0 \text{ V}$	P-Ch	-0.9	-1.2	
Dynamic^a						
Total Gate Charge	Q_g	N-Channel $V_{DS} = 6 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 5.0 \text{ A}$ P-Channel $V_{DS} = -6 \text{ V}, V_{GS} = -4.5 \text{ V}, I_D = -3.2 \text{ A}$	N-Ch	10	20	nC
Gate-Source Charge	Q_{gs}		P-Ch	8	20	
Gate-Drain Charge	Q_{gd}		N-Ch	2.6		
Turn-On Delay Time	$t_{d(\text{on})}$		P-Ch	1.6		
Rise Time	t_r		N-Ch	3.7		
Turn-Off Delay Time	$t_{d(\text{off})}$		P-Ch	3.5		
Fall Time	t_f	N-Channel $V_{DD} = 6 \text{ V}, R_L = 6 \Omega$ $I_D \cong 1 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_G = 6 \Omega$ P-Channel $V_{DD} = -6 \text{ V}, R_L = 6 \Omega$ $I_D \cong -1 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_G = 6 \Omega$	N-Ch	13	30	ns
Source-Drain Reverse Recovery Time	t_{rr}		P-Ch	22	40	
			N-Ch	9	40	
			P-Ch	43	80	
			N-Ch	30	60	
			P-Ch	35	70	
		$I_F = 5.0 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	N-Ch	9	30	
			P-Ch	20	40	
		$I_F = -2.0 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	N-Ch	100	150	
			P-Ch	75	100	

Notes

- a. For design aid only; not subject to production testing.
b. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

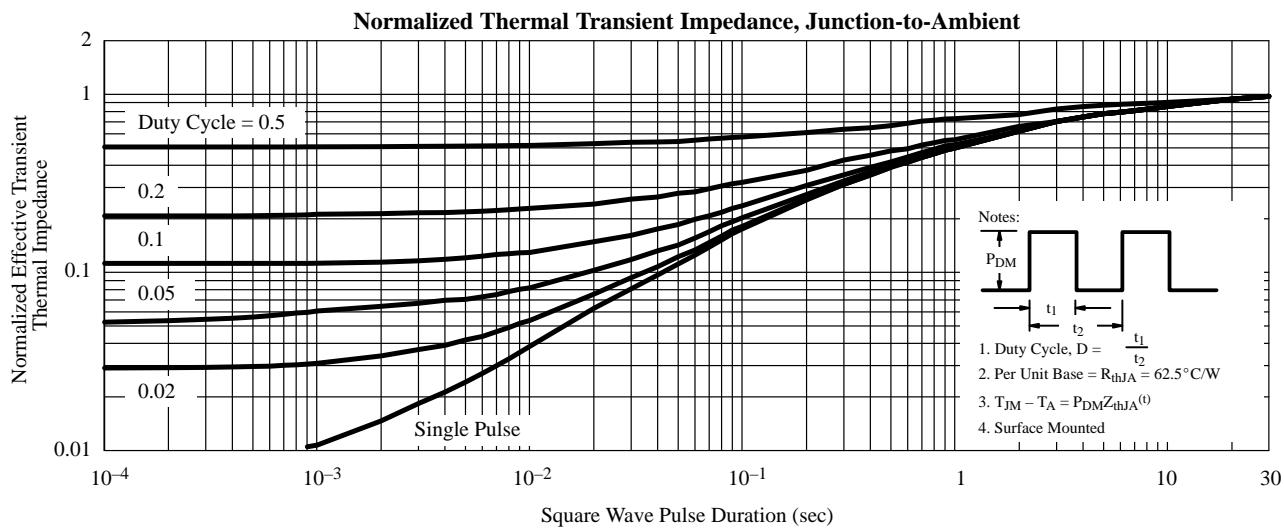
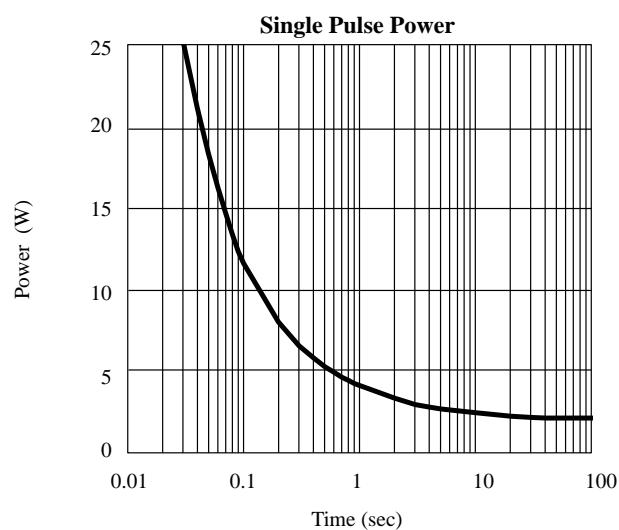
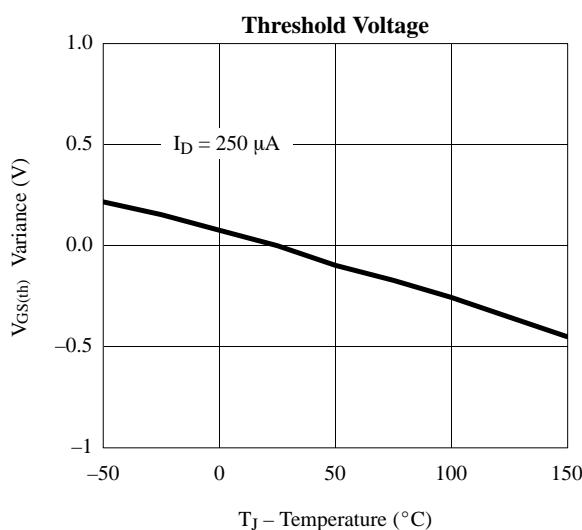
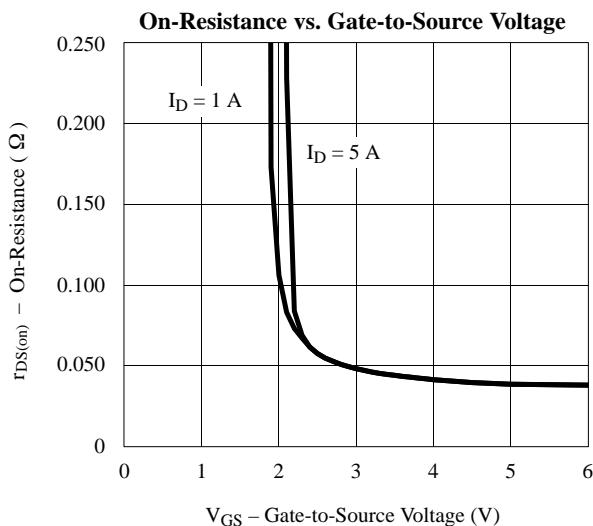
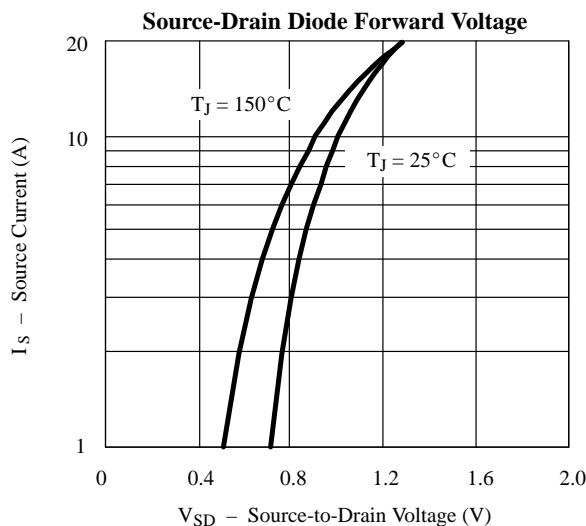
Typical Characteristics (25°C Unless Noted)

N-Channel



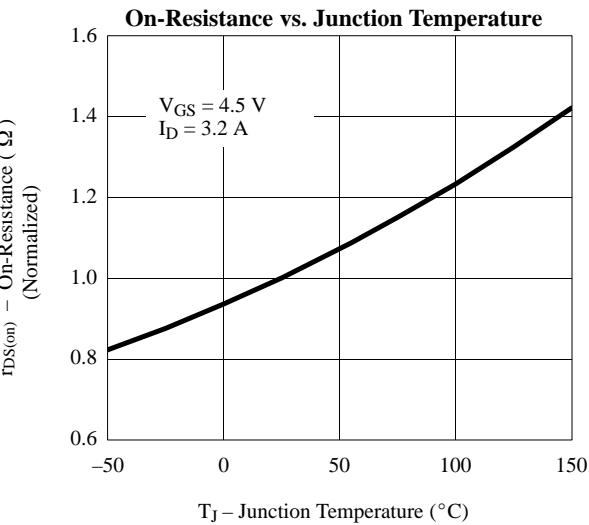
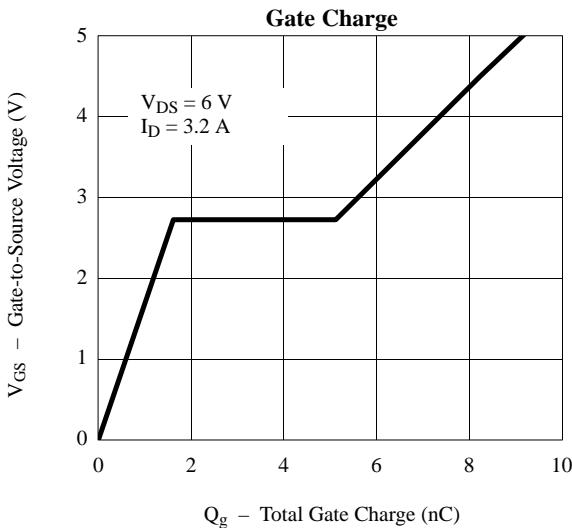
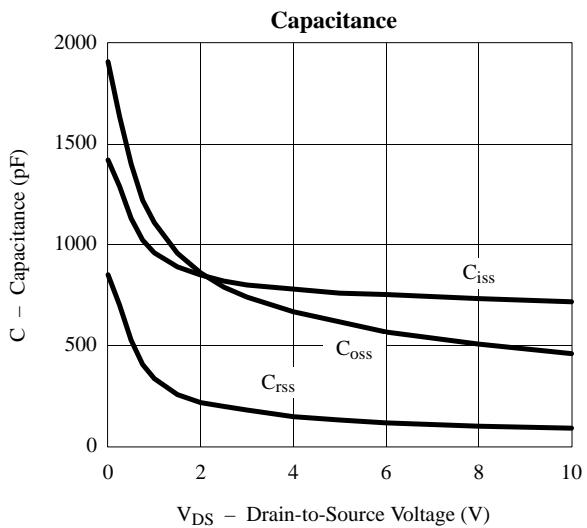
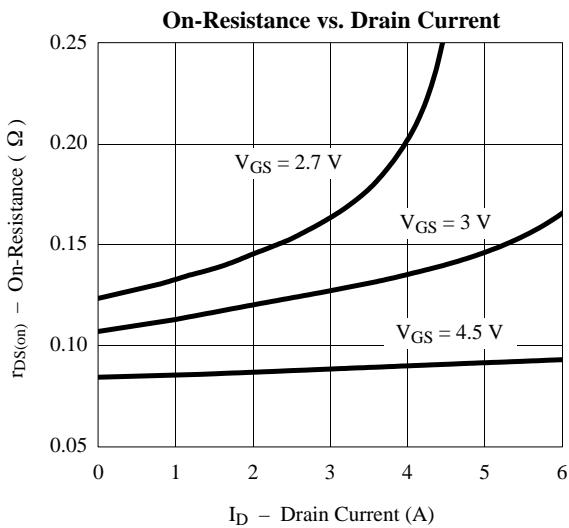
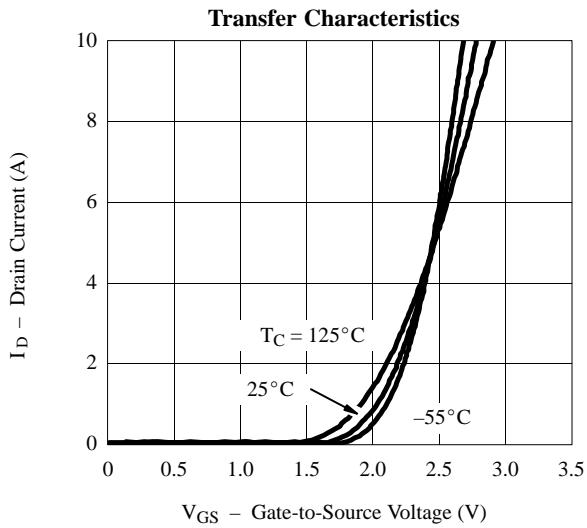
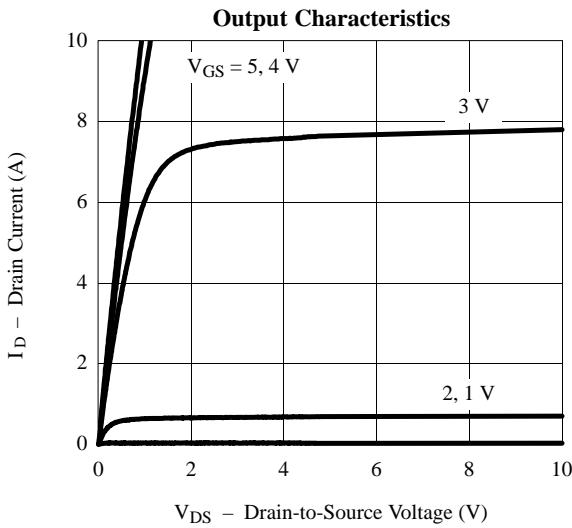
Typical Characteristics (25°C Unless Noted)

N-Channel



Typical Characteristics (25°C Unless Noted)

P-Channel



Typical Characteristics (25°C Unless Noted)

P-Channel

