N-Channel Enhancement-Mode MOSFET Transistors

PRODUCT SUMMARY				
Part Number	**$V_{(BR)DSS}$ Min (V)**	**$r_{DS(on)}$ Max (Ω)**	**$V_{GS(th)}$ (V)**	**I_D (A)**
TN0201L	20	1.2 @ V_{GS} = 10 V	0.5 to 2	0.64
TN0401L	40	1.2 @ V_{GS} = 10 V	0.5 to 2	0.64
VN0300L	30	1.2 @ V_{GS} = 10 V	0.8 to 2.5	0.64
VN0300LS	30	1.2 @ V_{GS} = 10 V	0.8 to 2.5	0.67

FEATURES

- Low On-Resistance: 0.85 Ω
- Low Threshold: 1.4 V
- Low Input Capacitance: 38 pF
- Fast Switching Speed: 9 ns
- Low Input and Output Leakage

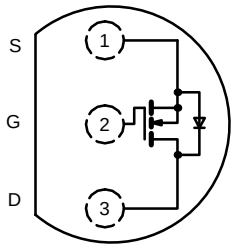
BENEFITS

- Low Offset Voltage
- Low-Voltage Operation
- Easily Driven Without Buffer
- High-Speed Circuits
- Low Error Voltage

APPLICATIONS

- Direct Logic-Level Interface: TTL/CMOS
- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories, Transistors, etc.
- Battery Operated Systems
- Solid-State Relays

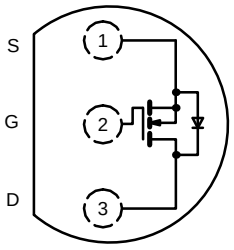
TO-226AA (TO-92)



Top View

TN0201L
TN0401L
VN0300L

TO-92S



Top View

VN0300LS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)							
Parameter		**Symbol**	**TN0201L**	**TN0401L**	**VN0300L**	**VN0300LS**	**Unit**
Drain-Source Voltage		V_{DS}	20	40	30	30	V
Gate-Source Voltage		V_{GS}	±20	±20	±30	±30	
Continuous Drain Current (T_J = 150°C)	T_A= 25°C	I_D	0.64	0.64	0.64	0.67	A
	T_A= 100°C		0.38	0.38	0.38	0.43	
Pulsed Drain Current[a]		I_{DM}	1.5	1.5	3	3	
Power Dissipation	T_A= 25°C	P_D	0.8	0.8	0.8	0.9	W
	T_A= 100°C		0.32	0.32	0.32	0.4	
Maximum Junction-to-Ambient		R_{thJA}	156	156	156	156	°C/W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150				°C

Notes
a. Pulse width limited by maximum junction temperature.

SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)

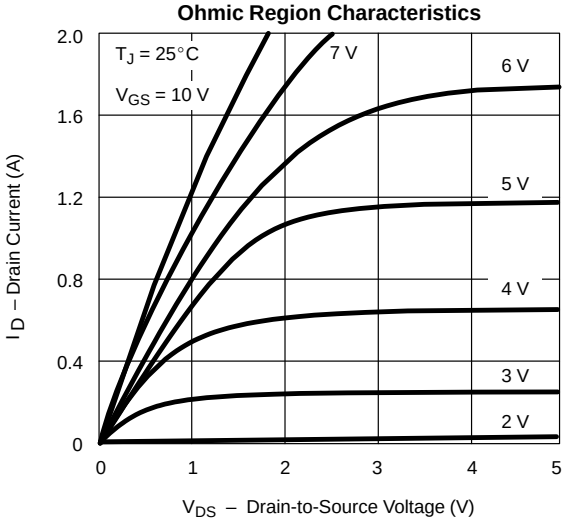
Parameter	Symbol	Test Conditions		Typ[a]	Limits TN0201L TN0401L Min	Limits TN0201L TN0401L Max	Limits VN0300L VN0300LS Min	Limits VN0300L VN0300LS Max	Unit
Static									
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	TN0201L	55	20				V
			TN0401L	55	40				
							30		
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 0.25 mA		1.4	0.5	2			
		V_{DS} = V_{GS}, I_D = 1 mA		1.5			0.8	2.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±10			nA
		V_{DS} = 0 V, V_{GS} = ±30 V						±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V						10	µA
			T_J = 125°C					500	
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V				1			
			T_J = 125°C			100			
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 4.5 V		0.9	0.25				A
		V_{DS} = 10 V, V_{GS} = 10 V		3.5	1		1		
Drain-Source On-Resistance[b]	$r_{DS(on)}$	V_{GS} = 3.5 V, I_D = 0.05 A		1.8		4			Ω
		V_{GS} = 5 V, I_D = 0.3 A		1.2				3.3	
		V_{GS} = 4.5 V, I_D = 0.25 A		1.4		2			
			T_J = 125°C	2.6		4			
		V_{GS} = 10 V, I_D = 1 A		0.85		1.2		1.2	
			T_J = 125°C	1.6				2.4	
Forward Transconductance[b]	g_{fs}	V_{DS} = 10 V, I_D = 0.5 A		500	200		200		mS
Dynamic									
Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz		38		60		100	pF
Output Capacitance	C_{oss}			33		50		95	
Reverse Transfer Capacitance	C_{rss}			8		15		25	
Switching[c]									
Turn-On Time	t_{ON}	V_{DD} = 15 V, R_L = 14 Ω, I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 25 Ω		10		30		30	ns
Turn-Off Time	t_{OFF}			13		30		30	

Notes
a. For DESIGN AID ONLY, not subject to production testing..
b. Pulse test: PW ≤ 300 µs duty cycle ≤ 2%.
c. Switching time is essentially independent of operating temperature.

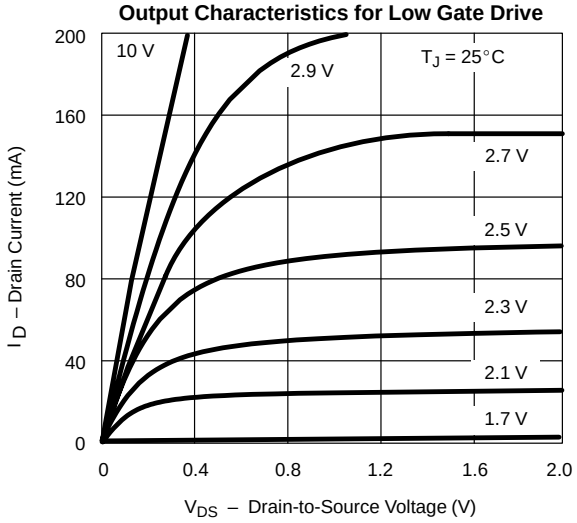
VNDQ03

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

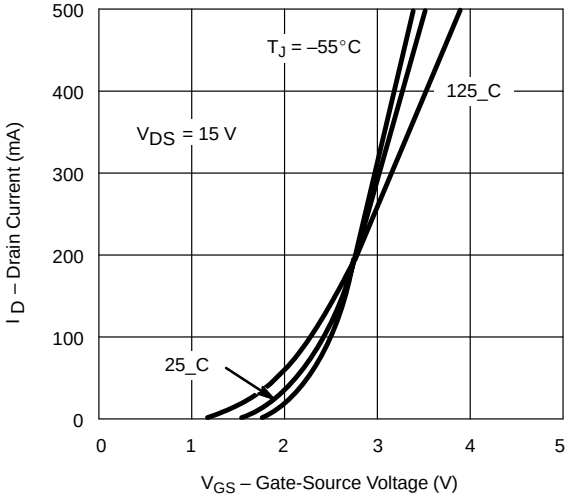
Ohmic Region Characteristics



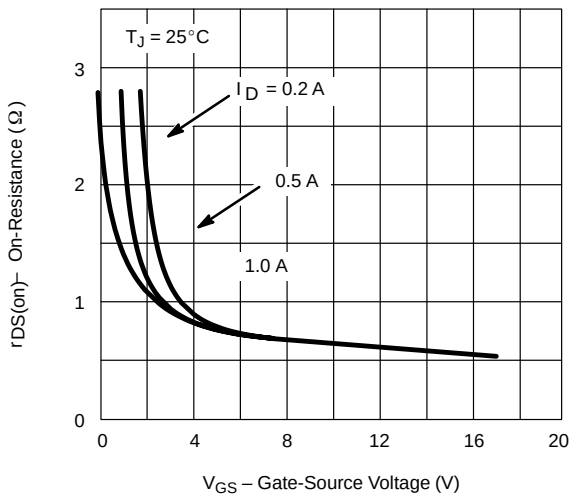
Output Characteristics for Low Gate Drive



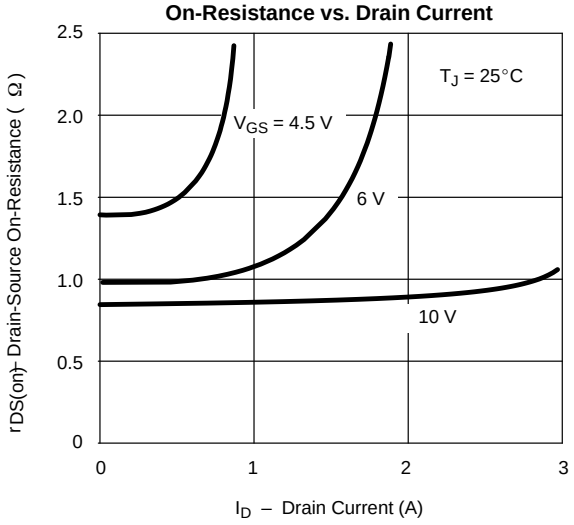
Transfer Characteristics



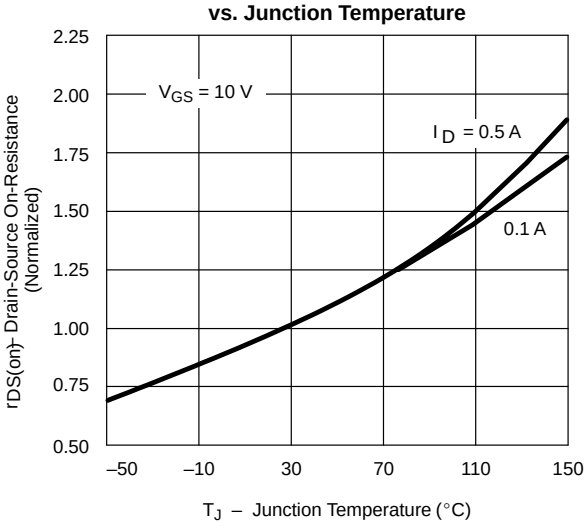
On-Resistance vs. Gate-to-Source Voltage



On-Resistance vs. Drain Current

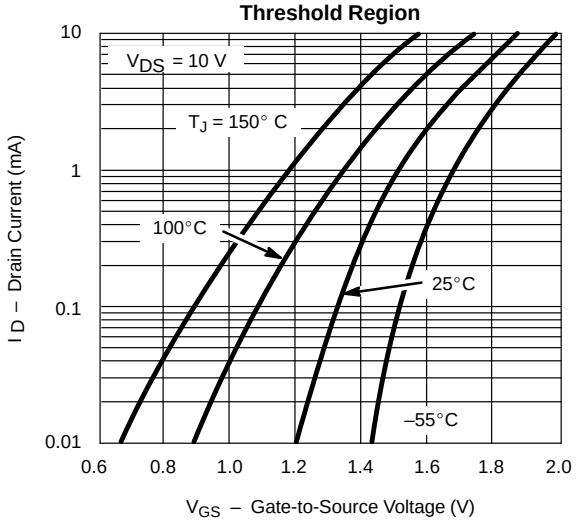


Normalized On-Resistance vs. Junction Temperature

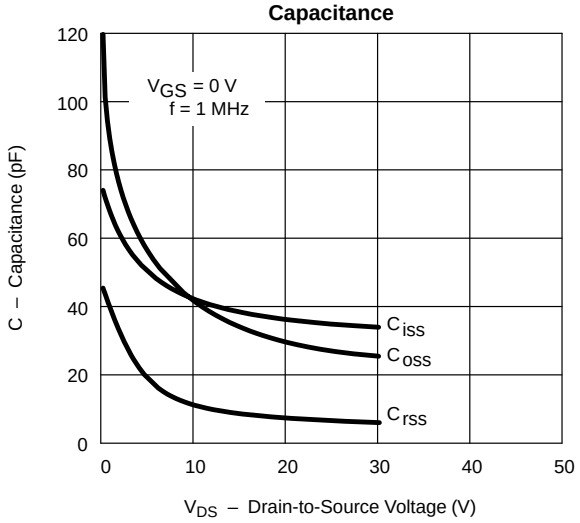


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

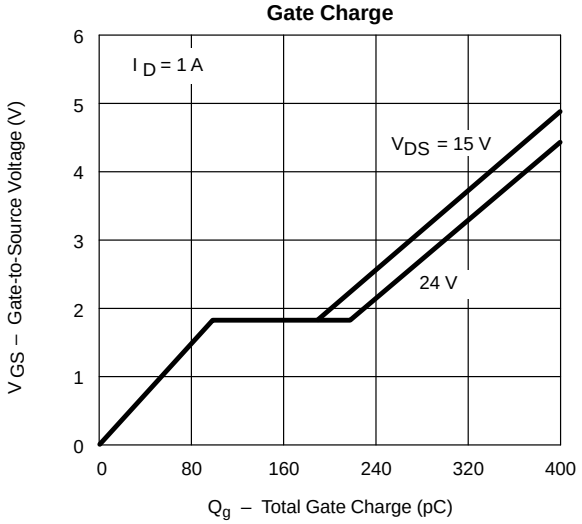
Threshold Region



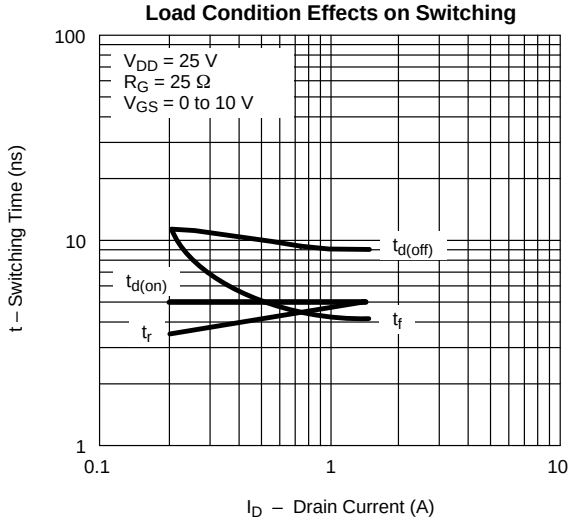
Capacitance



Gate Charge



Load Condition Effects on Switching



Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-226AA)