TN2435
Low Threshold

Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-243AA*	Die**
350V	6.0Ω	1.0A	TN2435N8	TN2435NW

* Same as SOT-89. Product supplied on 2000 piece carrier tape reels.
** Die in wafer form.

Product marking for TO-243AA:
TN4D❋
where ❋ = 2-week alpha date code

Features

- ❏ High input impedance
- ❏ Low input capacitance
- ❏ Fast switching speeds
- ❏ Free from secondary breakdown
- ❏ Low input and output leakage
- ❏ Complementary N- and P-channel devices

Applications

- ❏ Logic level interfaces
- ❏ Solid state relays
- ❏ Power Management
- ❏ Analog switches
- ❏ Ringers
- ❏ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

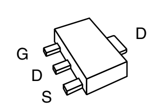
* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Option



TO-243AA
(SOT-89)

Note: See Package Outline section for dimensions.

11/12/01

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_A = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-243AA	365mA	1.8A	1.6W†	15	78†	365mA	1.8A

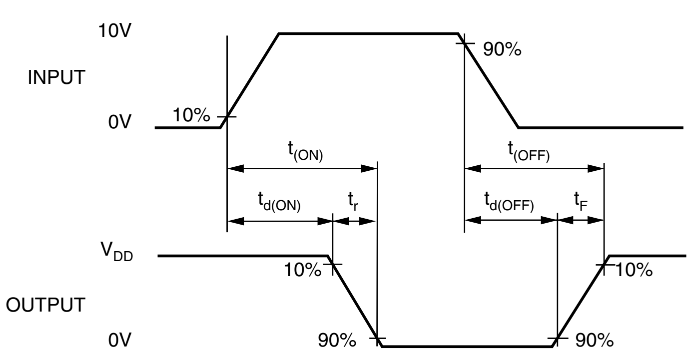
* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

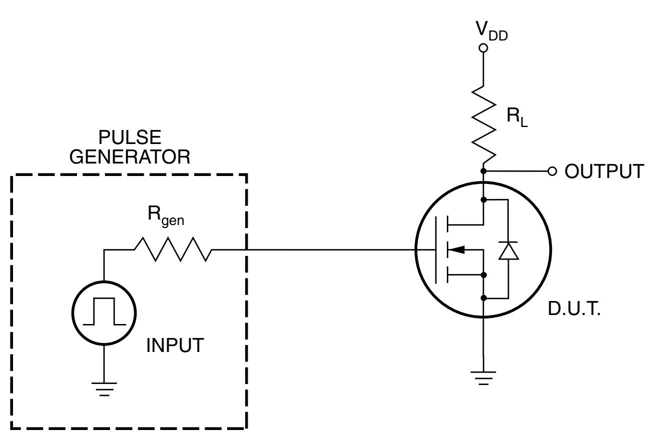
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	350			V	$V_{GS} = 0V$, $I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	0.8			V	$V_{GS} = V_{DS}$, $I_D = 1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-5.5	mV/°C	$V_{GS} = V_{DS}$, $I_D = 1.0mA$
I_{GSS}	Gate Body Leakage			100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current			10	µA	$V_{GS} = 0V$, V_{DS} = Max Rating
				1.0	mA	$V_{GS} = 0V$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current	0.5			A	$V_{GS} = 4.5V$, $V_{DS} = 25V$
		1.0				$V_{GS} = 10V$, $V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to Source ON-State Resistance			15.0	Ω	$V_{GS} = 3.0V$, $I_D = 150mA$
				10.0		$V_{GS} = 4.5V$, $I_D = 250mA$
				6.0		$V_{GS} = 10V$, $I_D = 750mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1.7	%/°C	$V_{GS} = 10V$, $I_D = 750mA$
G_{FS}	Forward Transconductance	125			m℧	$V_{DS} = 25V$, $I_D = 350mA$
C_{ISS}	Input Capacitance		125	200	pF	$V_{GS} = 0V$, $V_{DS} = 25V$ f = 1.0MHz
C_{OSS}	Common Source Output Capacitance		25	70		
C_{RSS}	Reverse Transfer Capacitance		8	25		
$t_{d(ON)}$	Turn-ON Delay Time		5	20	ns	$V_{DD} = 25V$, $I_D = 750mA$ $R_{GEN} = 25\Omega$
t_r	Rise Time		10	20		
$t_{d(OFF)}$	Turn-OFF Delay Time		28	40		
t_f	Fall Time		10	30		
V_{SD}	Diode Forward Voltage Drop			1.5	V	$V_{GS} = 0V$, $I_{SD} = 750mA$
t_{rr}	Reverse Recovery Time		300		ns	$V_{GS} = 0V$, $I_{SD} = 750mA$

Notes:
1.All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2.All A.C. parameters sample tested.

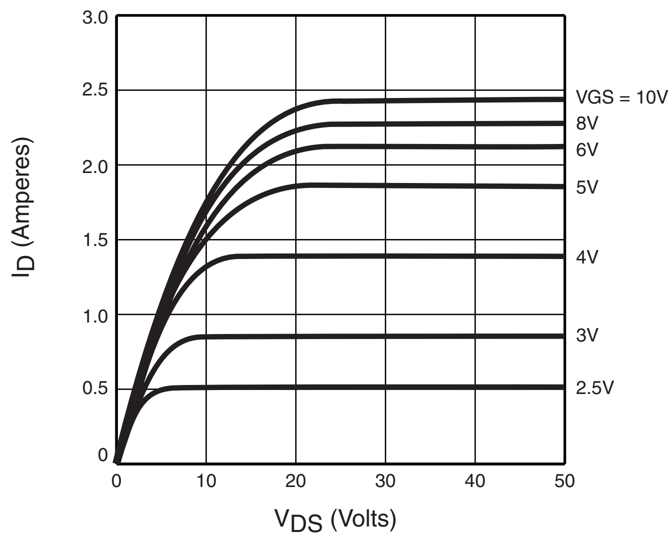
Switching Waveforms and Test Circuit



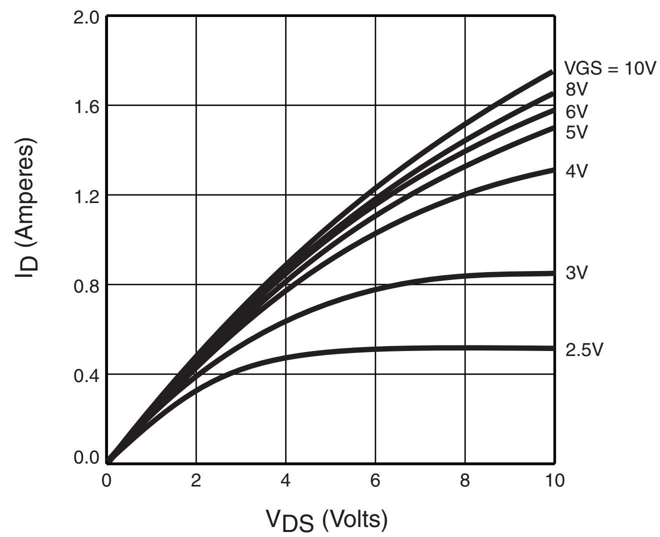


Typical Performance Curves

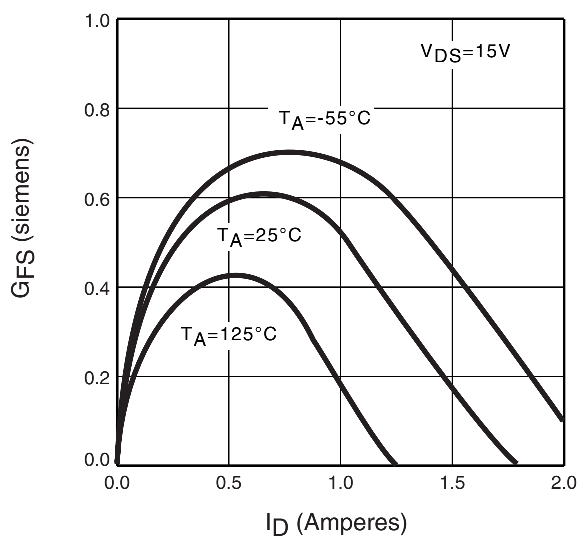
Output Characteristics



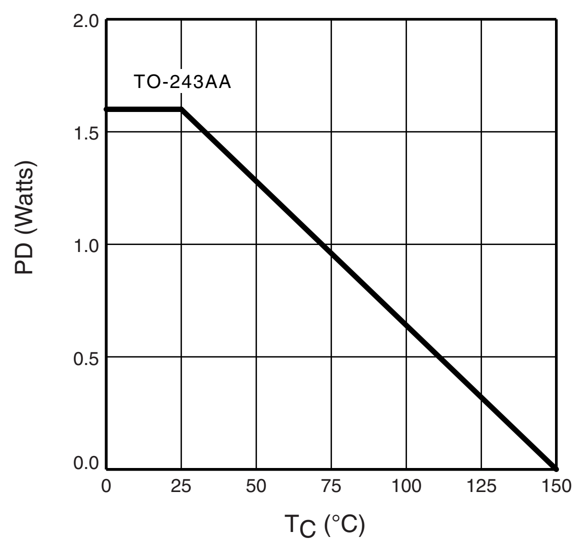
Saturation Characteristics



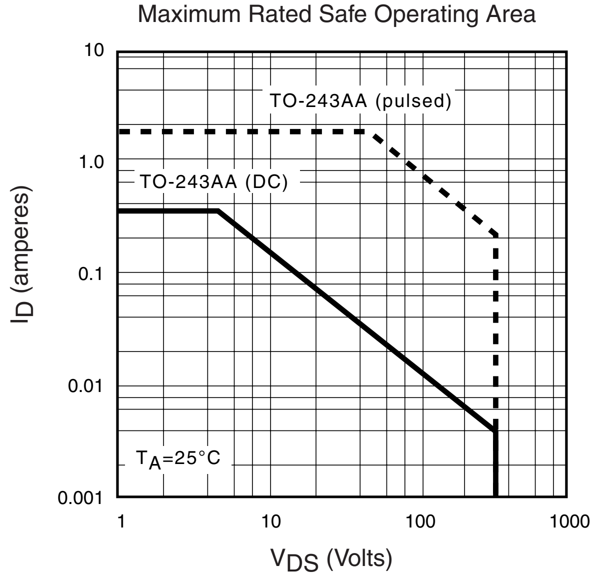
Transconductance vs. Drain Current



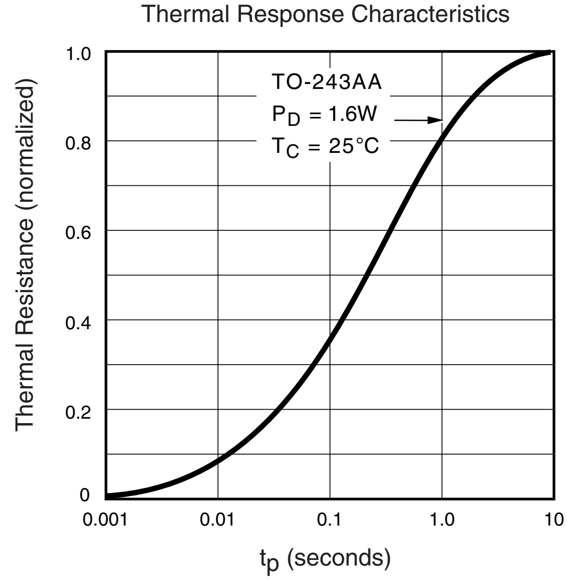
Power Dissipation vs. Case Temperature



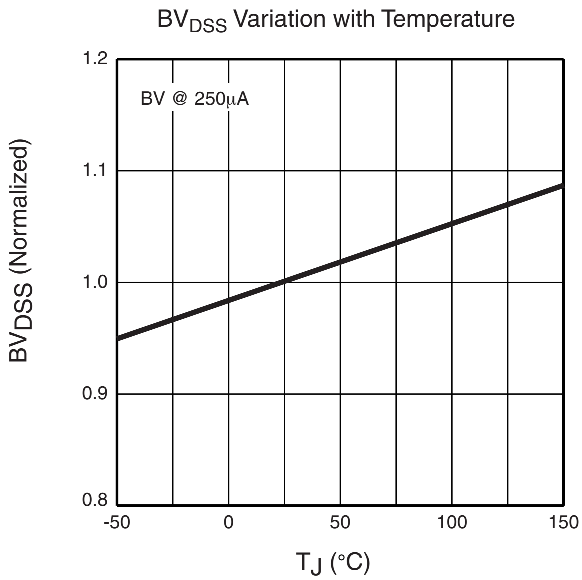
Maximum Rated Safe Operating Area

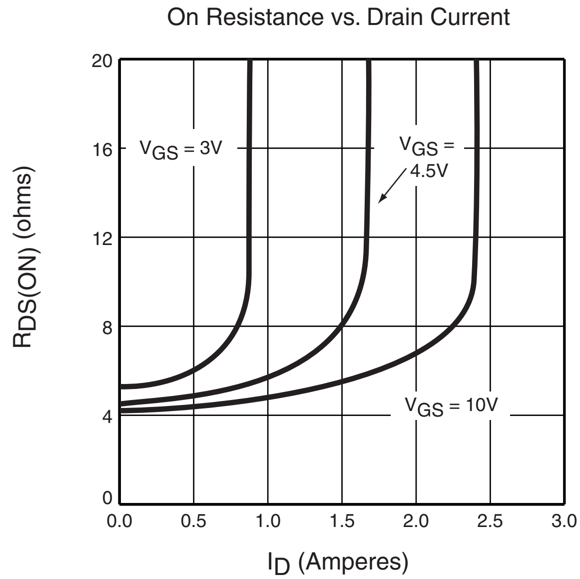


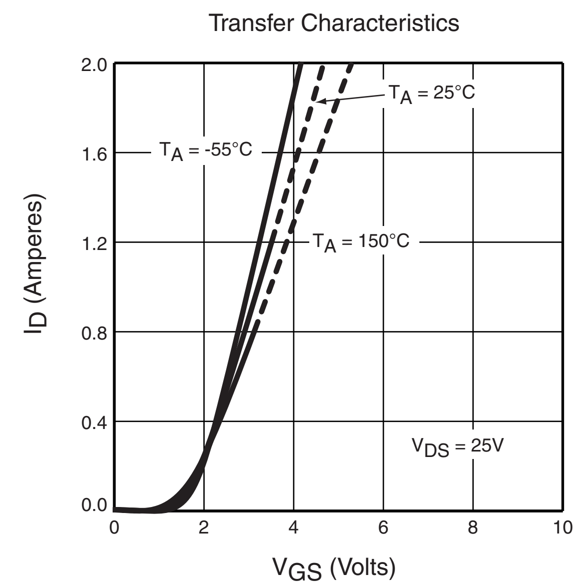
Thermal Response Characteristics

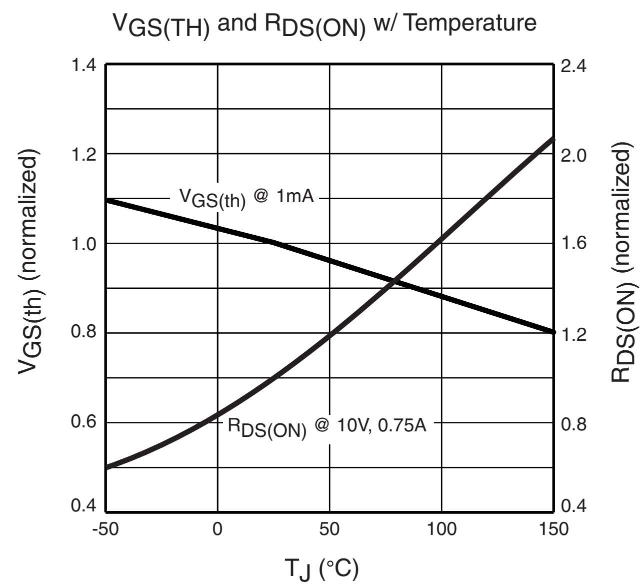


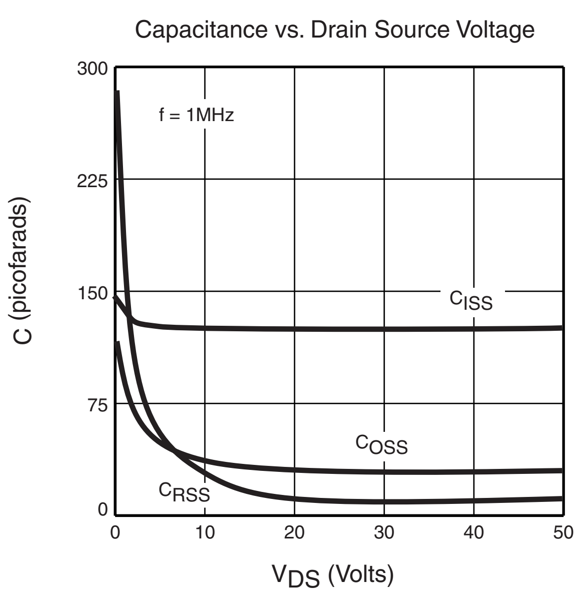
Typical Performance Curves

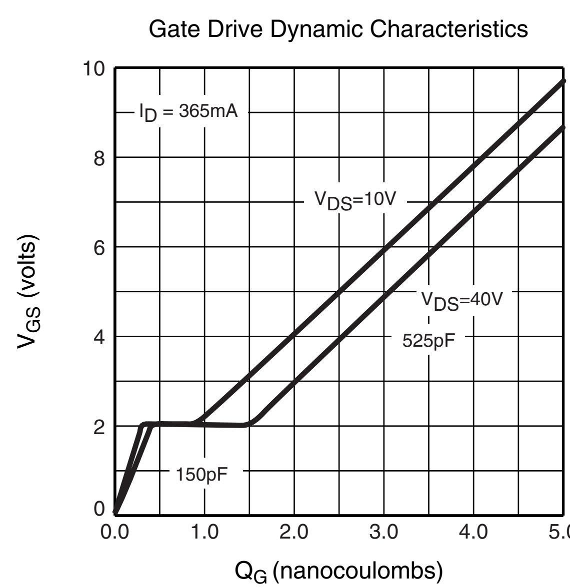












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