



P-Channel Enhancement-Mode Vertical DMOS FET Quad Array

Ordering Information

BV _{DSS} / BV _{DGS}	R _{DS (ON)} Max	Order Number / Package
		SOW-20*
-40V	2.0Ω	TP0604WG

* Same as SO-20 with 300 mil wide body.

Features

- 4 independent channels
- 4 electrically isolated die
- Commercial and Military versions available
- Free from secondary breakdown
- Low power drive requirement
- Low C_{ISS} and fast switching speeds
- High input impedance and high gain

Applications

- Telecom switches
- Logic level interfaces
- Battery operated systems
- Photo voltaic drives
- Solid state relays
- Motor controls

Absolute Maximum Ratings

Drain-to-Source Voltage	BV _{DSS}
Drain-to-Gate Voltage	BV _{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

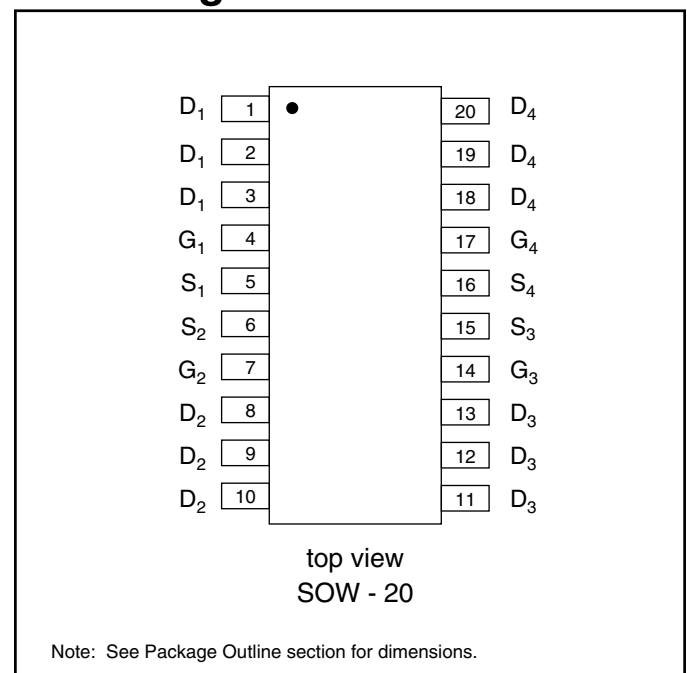
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) DMOS FET arrays utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex quad arrays use four independent DMOS transistors. They are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Pin Configuration



Thermal Characteristics

Package	I_D (continuous)* (single die)	I_D (pulsed)	Power Dissipation @ $T_A = 25^\circ\text{C}$	θ_{jc} $^\circ\text{C/W}$	θ_{ja} $^\circ\text{C/W}$	I_{DR}^* (single die)	I_{DRM}
SOW-20	-0.6A	-2.0A	1.5W	—	84	-0.6A	-2.0A

* I_D (continuous) is limited by max rated T_j .

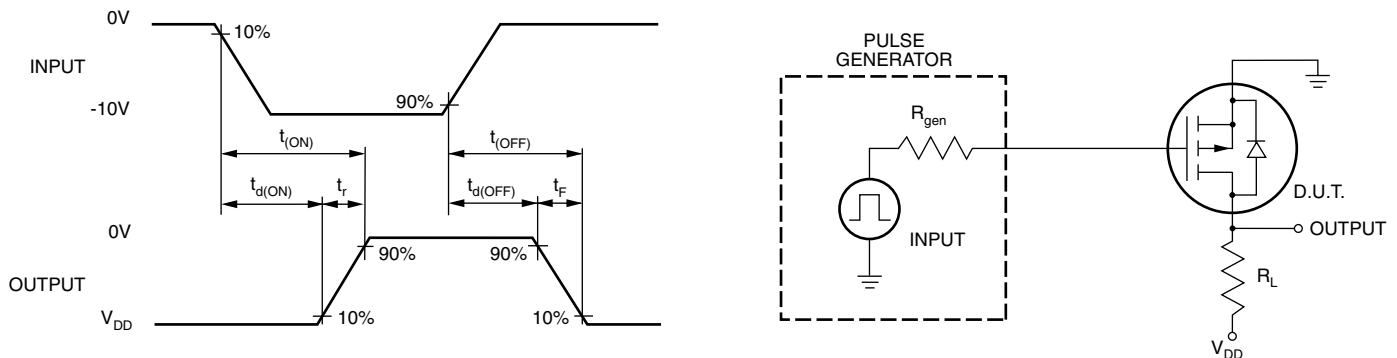
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-40			V	$V_{GS} = 0V, I_D = -2.0mA$
$V_{GS(th)}$	Gate Threshold Voltage	-1.0		-2.4	V	$V_{GS} = V_{DS}, I_D = -1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		-3.0	-4.5	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = -1.0mA$
I_{GSS}	Gate Body Leakage			-100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current			-10	μA	$V_{GS} = 0V, V_{DS} = \text{Max Rating}$
				-1.0	mA	$V_{GS} = 0V, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current	-0.4	-0.6		A	$V_{GS} = -5V, V_{DS} = -20V$
		-2.0	-3.3			$V_{GS} = -10V, V_{DS} = -20V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		2.0	3.5	Ω	$V_{GS} = -5V, I_D = -250mA$
			1.5	2.0		$V_{GS} = -10V, I_D = -1.0A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature		0.75	1.2	%/ $^\circ\text{C}$	$V_{GS} = -10V, I_D = -1.0A$
G_{FS}	Forward Transconductance	0.4	0.6		S	$V_{DS} = -20V, I_D = -1.0A$
C_{ISS}	Input Capacitance		95	150	pF	$V_{GS} = 0V, V_{DS} = -20V$ $f = 1 \text{ MHz}$
C_{OSS}	Common Source Output Capacitance		85	120		
C_{RSS}	Reverse Transfer Capacitance		35	60		
$t_{d(ON)}$	Turn-ON Delay Time		5.0	8	ns	$V_{DD} = -20V$ $I_D = -1.0A$ $R_{GEN} = 25\Omega$
t_r	Rise Time		7.0	18		
$t_{d(OFF)}$	Turn-OFF Delay Time		10	15		
t_f	Fall Time		6.0	19		
V_{SD}	Diode Forward Voltage Drop		-1.3	-2.0	V	$V_{GS} = 0V, I_{SD} = -1.5A$
t_{rr}	Reverse Recovery Time		300		ns	$V_{GS} = 0V, I_{SD} = -1.5A$

Notes:

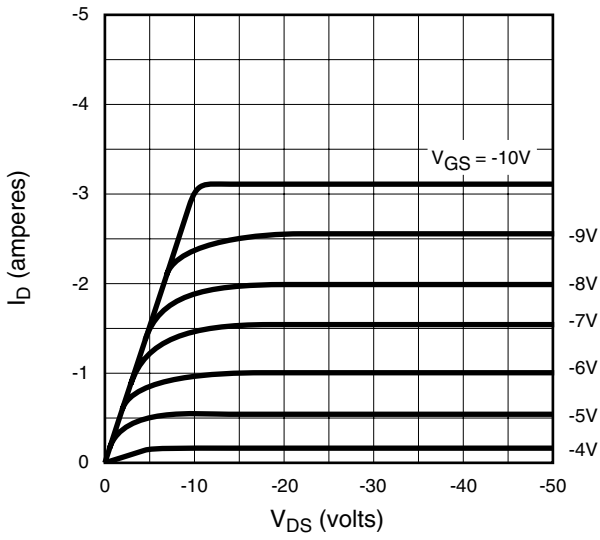
- All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

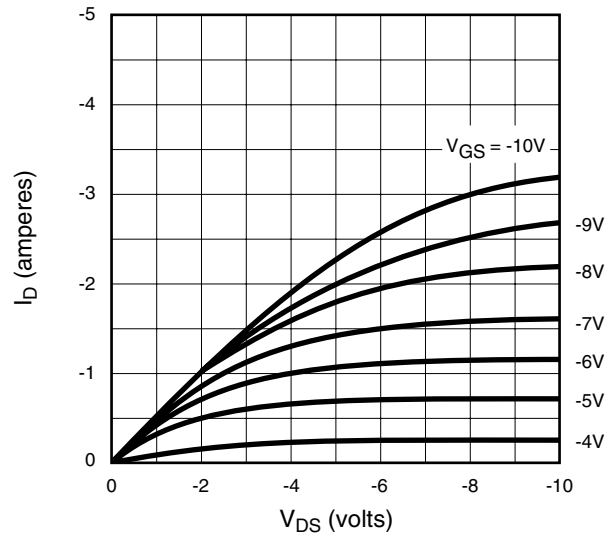


Typical Performance Curves

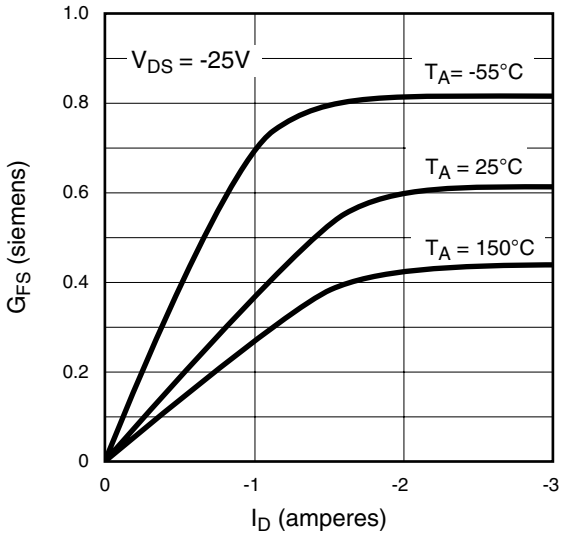
Output Characteristics



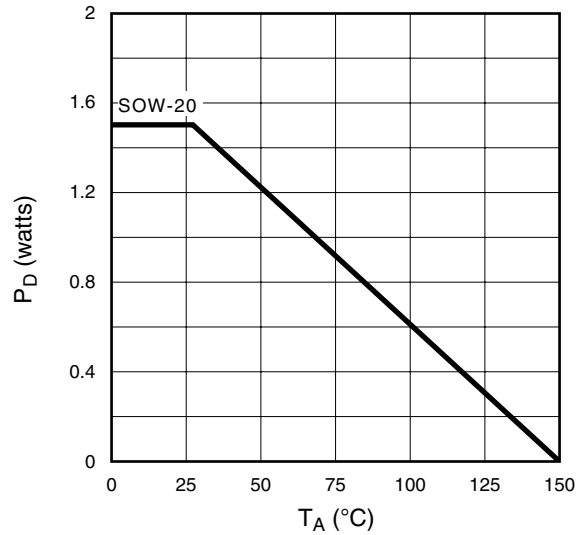
Saturation Characteristics



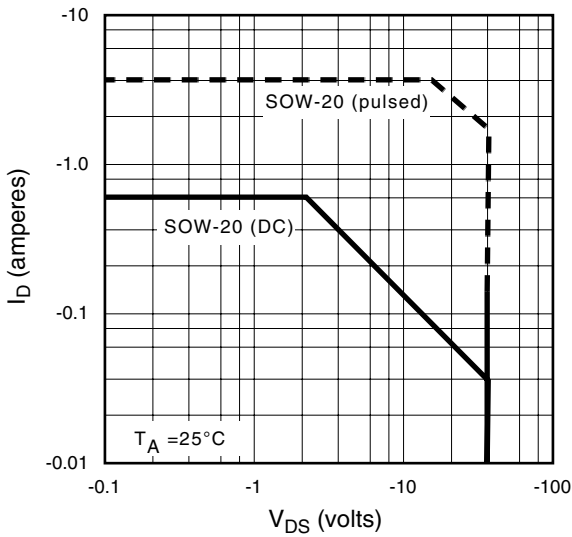
Transconductance vs. Drain Current



Power Dissipation vs. Ambient Temperature

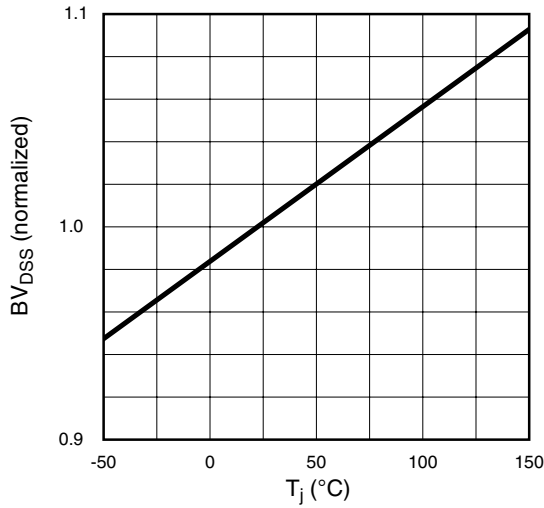


Maximum Rated Safe Operating Area

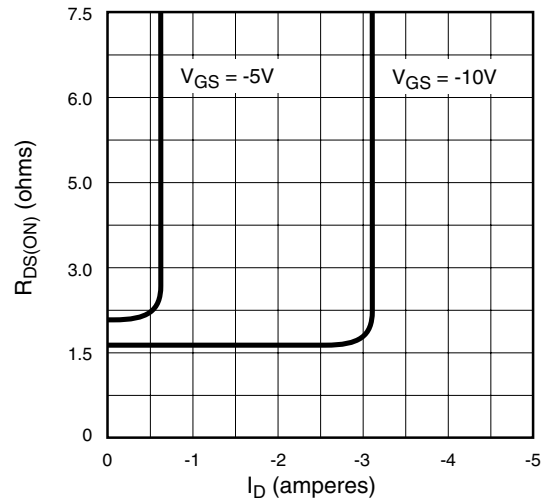


Typical Performance Curves

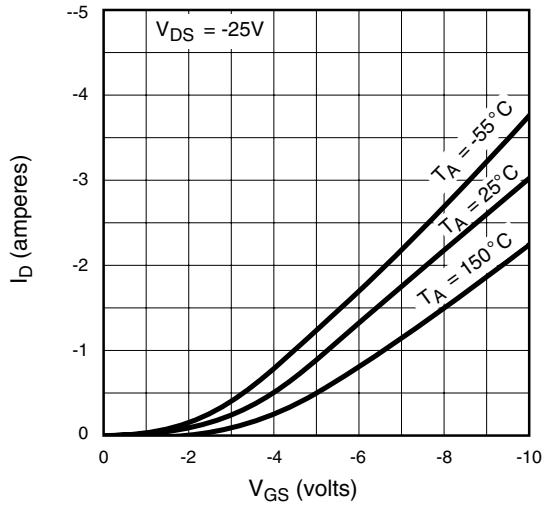
BV_{DSS} Variation with Temperature



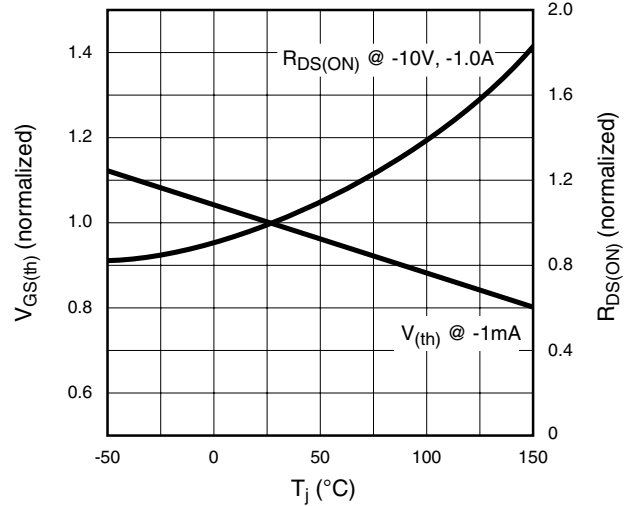
On-Resistance vs. Drain Current



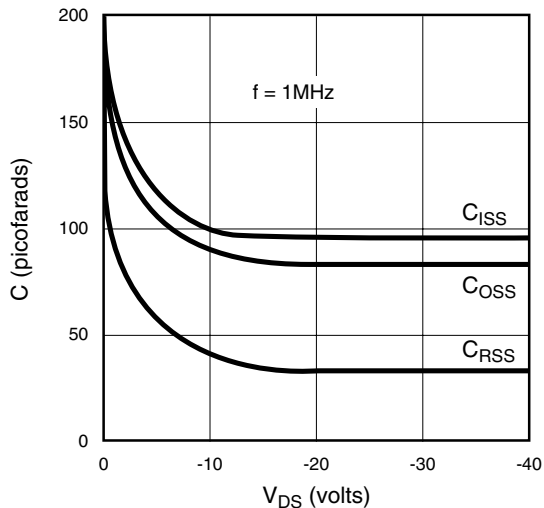
Transfer Characteristics



V_(th) and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

