



P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV _{DSS} /	R _{DS(ON)}	I _{D(ON)}	V _{GS(th)}	Order Number / Package			
BV _{DGS}	(max)	(min)	(max)	TO-92			
-60V	3.5Ω	-1.5A	-2.4V	TP0606N3			

Features

- Low threshold -2.4V max
- High input impedance
- Low input capacitance 80pF typical
- → Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage
- Complementary N- and P-channel devices

Applications

- ☐ Logic level interfaces ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drives
- Analog switches
- General purpose line drivers
- Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV _{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

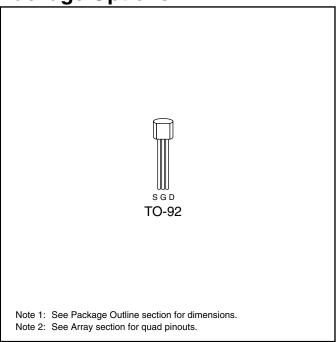
^{*} Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Thermal Characteristics

Package	I _D (continuous)*	I _D (pulsed)	Power Dissipation @ T _C = 25°C	$ heta_{ extsf{jc}}$ $^{\circ}$ C/W	θ _{ja} °C/W	I _{DR} *	I _{DRM}
TO-92	0.32A	-3.5A	1W	125	170	0.32A	-3.5A

 $^{^*}$ I_D (continuous) is limited by max rated T_i.

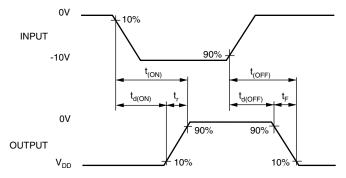
Electrical Characteristics (@ 25°C unless otherwise specified)

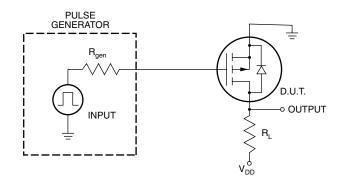
Symbol	Parameter	Min	Тур	Max	Unit	Conditions	
BV _{DSS}	Drain-to-Source Breakdown Voltage	-60			V	$V_{GS} = 0V, I_{D} = -2.0 \text{mA}$	
V _{GS(th)}	Gate Threshold Voltage	-1.0		-2.4	V	$V_{GS} = V_{DS}$, $I_D = -1.0$ mA	
$\Delta V_{GS(th)}$	Change in V _{GS(th)} with Temperature			-5.0	mV/°C	$V_{GS} = V_{DS}$, $I_D = -1.0$ mA	
I _{GSS}	Gate Body Leakage			-100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
I _{DSS}	Zero Gate Voltage Drain Current			-10	μΑ	$V_{GS} = 0V$, $V_{DS} = Max$ Rating	
				-1.0	mA	$V_{GS} = 0V$, $V_{DS} = 0.8$ Max Rating $T_A = 125$ °C	
I _{D(ON)}	ON-State Drain Current	-0.4	-0.6			$V_{GS} = -5V, V_{DS} = -25V$	
		-1.5	-2.5	1	A	$V_{GS} = -10V, V_{DS} = -25V$	
R _{DS(ON)}	Static Drain-to-Source		5.0	7.0	Ω	$V_{GS} = -5V, I_{D} = -250 \text{mA}$	
	ON-State Resistance		3.0	3.5		$V_{GS} = -10V, I_D = -0.75A$	
$\Delta R_{DS(ON)}$	Change in R _{DS(ON)} with Temperature			1.7	%/°C	$V_{GS} = -10V, I_D = -0.75A$	
G _{FS}	Forward Transconductance	300	400		mъ	$V_{DS} = -25V, I_{D} = -0.75A$	
C _{ISS}	Input Capacitance		80	150			
C _{OSS}	Common Source Output Capacitance		50	85	pF	$V_{GS} = 0V, V_{DS} = -25V$ f = 1 MHz	
C _{RSS}	Reverse Transfer Capacitance		15	35			
t _{d(ON)}	Turn-ON Delay Time			10		$V_{DD} = -25V$ $I_{D} = -1.0A$ $R_{GEN} = 25\Omega$	
t _r	Rise Time			15	ns		
t _{d(OFF)}	Turn-OFF Delay Time			20]		
t _f	Fall Time			15			
V _{SD}	Diode Forward Voltage Drop			-1.8	V	$V_{GS} = 0V, I_{SD} = -1.0A$	
t _{rr}	Reverse Recovery Time		300		ns	$V_{GS} = 0V, I_{SD} = -1.0A$	

Notes:

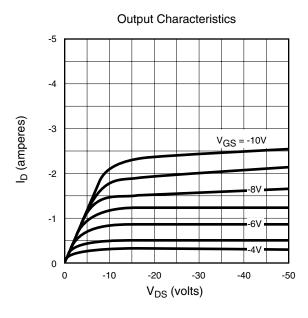
- 1. All D.C. parameters 100% tested at 25° C unless otherwise stated. (Pulse test: $300 \mu s$ pulse, 2% duty cycle.)
- 2. All A.C. parameters sample tested.

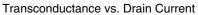
Switching Waveforms and Test Circuit

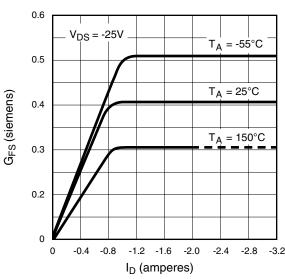




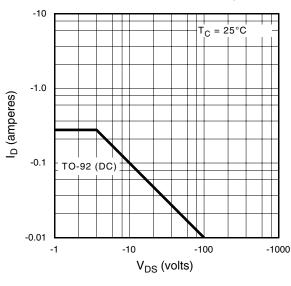
Typical Performance Curves



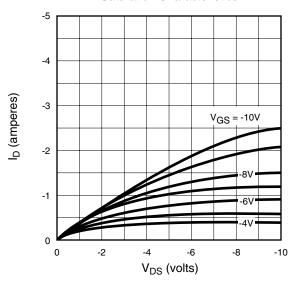




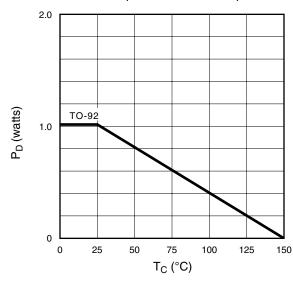
Maximum Rated Safe Operating Area



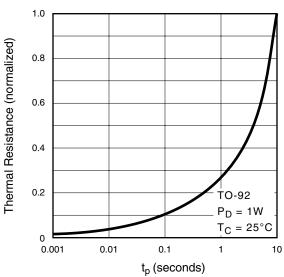
Saturation Characteristics



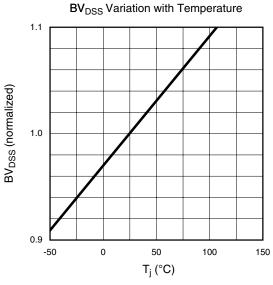
Power Dissipation vs. Case Temperature



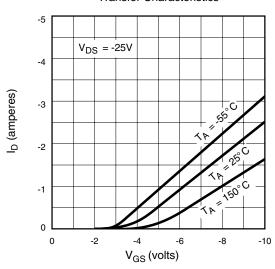
Thermal Response Characteristics



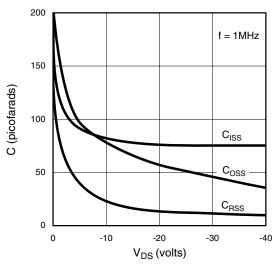
Typical Performance Curves



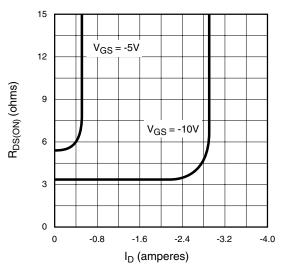




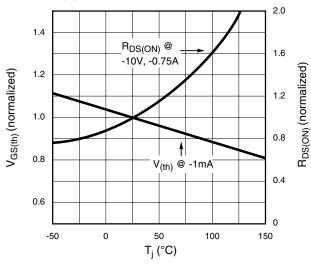
Capacitance vs. Drain-to-Source Voltage



On-Resistance vs. Drain Current



$V_{(th)}$ and R_{DS} Variation with Temperature



Gate Drive Dynamic Characteristics

