

N-Channel Enhancement-Mode Vertical DMOS FET

Ordering Information

BV _{DSS} /	R _{DS(ON)}	I _{D(ON)}	Order Number / Package
BV _{DGS}	(max)	(min)	TO-92
40V	3.0Ω	2.0A	VN0104N3
60V	3.0Ω	2.0A	VN0106N3

Features

- ☐ Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor controls
- ☐ Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

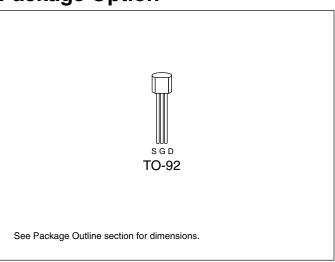
^{*} Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Option



Thermal Characteristics

Package	I _D (continuous)*	I _D (pulsed)	Power Dissipation @ T _C = 25°C	$ heta_{ extsf{jc}}$ $^{\circ}$ C/W	θ _{ja} °C/W	I _{DR} *	I _{DRM}
TO-92	350mA	2.0A	1.0W	125	170	350mA	2.0A

^{*} In (continuous) is limited by max rated Ti.

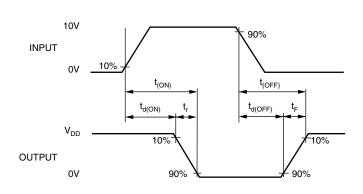
Electrical Characteristics (@ 25°C unless otherwise specified)

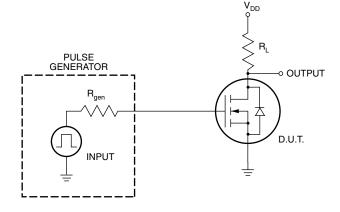
Symbol	Parameter		Min	Тур	Max	Unit	Conditions	
BV _{DSS}	Drain-to-Source Breakdown Voltage	VN0106	60			V	$V_{GS} = 0V, I_D = 1mA$	
		VN0104	40				GS - GV, ID - IIIII	
V _{GS(th)}	Gate Threshold Voltage	•	0.8		2.4	V	$V_{GS} = V_{DS}$, $I_D = 1mA$	
$\Delta V_{GS(th)}$	Change in V _{GS(th)} with Temperature			-3.8	-5.5	mV/°C	$V_{GS} = V_{DS}$, $I_D = 1mA$	
I _{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
I _{DSS}	Zero Gate Voltage Drain Current				1		V _{GS} = 0V, V _{DS} = Max Rating	
					100	μΑ	$V_{GS} = 0V$, $V_{DS} = 0.8$ Max Rating $T_A = 125$ °C	
I _{D(ON)}	ON-State Drain Current		0.5	1.0		Α	$V_{GS} = 5V, V_{DS} = 25V$	
			2.0	2.5			V _{GS} = 10V, V _{DS} = 25V	
R _{DS(ON)}	Static Drain-to-Source ON-State Resistance			3.0	5.0	Ω	$V_{GS} = 5V, I_{D} = 250mA$	
				2.5	3.0		$V_{GS} = 10V, I_{D} = 1A$	
$\Delta R_{DS(ON)}$	Change in R _{DS(ON)} with Temperature			0.70	1	%/°C	V _{GS} = 10V, I _D = 1A	
G _{FS}	Forward Transconductance		300	450		m℧	$V_{DS} = 25V, I_{D} = 0.5A$	
C _{ISS}	Input Capacitance			55	65		$V_{GS} = 0V, V_{DS} = 25V$ f = 1 MHz	
C _{OSS}	Common Source Output Capacitance			20	25	pF		
C _{RSS}	Reverse Transfer Capacitance			5	8			
t _{d(ON)}	Turn-ON Delay Time			3	5		$V_{DD} = 25V$	
t _r	Rise Time			5	8	ns		
t _{d(OFF)}	Turn-OFF Delay Time			6	9		$I_D = 1A$ $R_{GEN} = 25\Omega$	
t _f	Fall Time			5	8]	GEN = 2011	
V _{SD}	Diode Forward Voltage Drop			1.2	1.8	V	V _{GS} = 0V, I _{SD} =1.0A	
t _{rr}	Reverse Recovery Time			400		ns	V _{GS} = 0V, I _{SD} =1.0A	

Notes

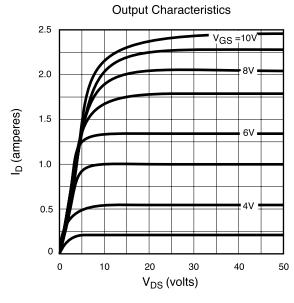
- 1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: $300\mu s$ pulse, 2% duty cycle.)
- 2. All A.C. parameters sample tested.

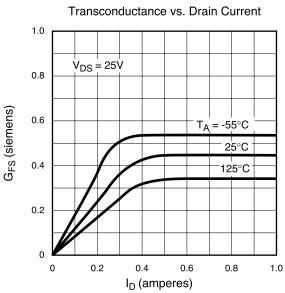
Switching Waveforms and Test Circuit

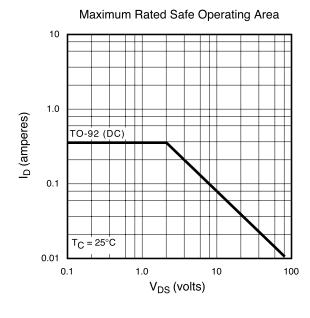


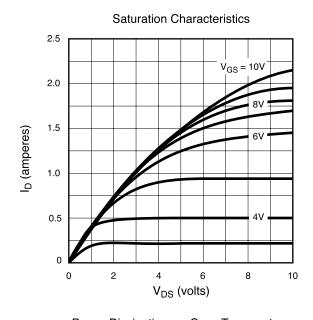


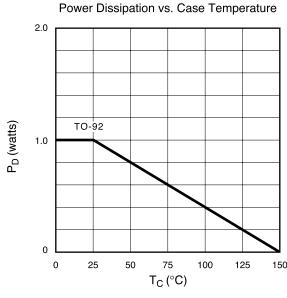
Typical Performance Curves

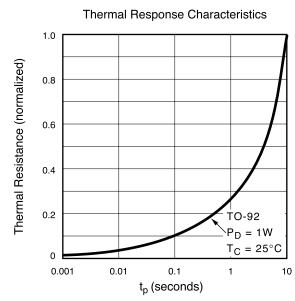




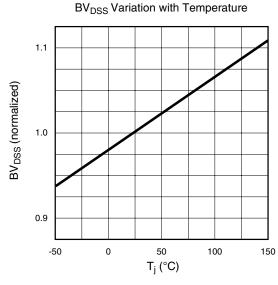


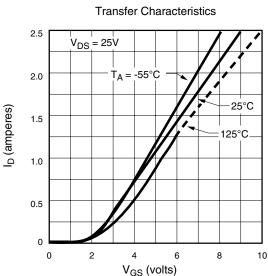


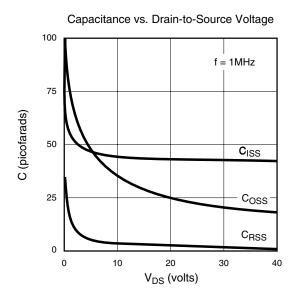


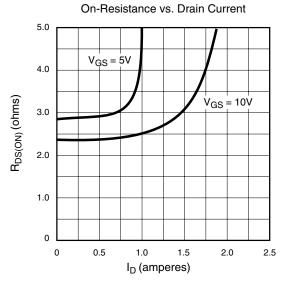


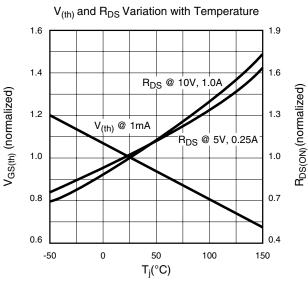
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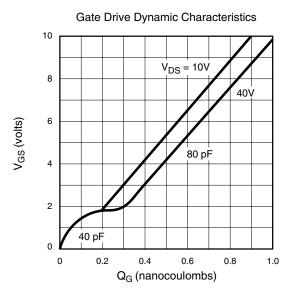












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