

P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

| ſ | BV _{DSS} / | R _{DS(ON)} | I _{D(ON)} | Order Number / Package | | |
|---|---------------------|---------------------|--------------------|------------------------|--|--|
| | BV _{DGS} | (max) | (min) | TO-92 | | |
| | -500V | 125Ω | -100mA | VP0550N3 | | |

Features

- □ Free from secondary breakdown
- Low power drive requirement
- □ Ease of paralleling
- □ Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- □ High input impedance and high gain
- □ Complementary N- and P-channel devices

Applications

- Motor controls
- Converters
- Amplifiers
- Switches

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- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

| Drain-to-Source Voltage | BV_{DSS} |
|-----------------------------------|-------------------|
| Drain-to-Gate Voltage | BV _{DGS} |
| Gate-to-Source Voltage | ± 20V |
| Operating and Storage Temperature | -55°C to +150°C |
| Soldering Temperature* | 300°C |

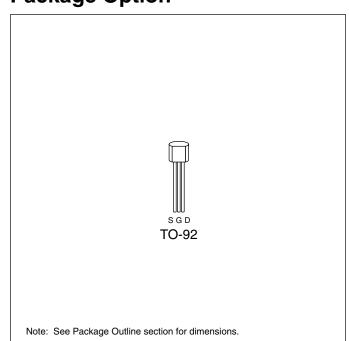
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Option



Supertex Inc. does not recommend the use of its products in life support applications and will not knowingly sell its products for use in such applications unless it receives an adequate "products liability indemnification insurance agreement." Supertex does not assume responsibility for use of devices described and limits its liability to the replacement of devices determined to be defective due to workmanship. No responsibility is assumed for possible omissions or inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications, refer to the Supertex website: http://www.supertex.com. For complete liability information on all Supertex products, refer to the most current databook or to the Legal/Disclaimer page on the Supertex website.

Thermal Characteristics

| Package | I _D (continuous)* | I _D (pulsed) | Power Dissipation @ T _C = 25°C | θ _{jc} °C/W | θ _{ja} °C/W | I _{DR} * | I _{DRM} |
|---------|------------------------------|-------------------------|--|-------------------------|-------------------------|-------------------|------------------|
| TO-92 | -54mA | -0.25A | 1W | 125 | 170 | -54mA | -0.25A |

* I_D (continuous) is limited by max rated T_i .

Electrical Characteristics (@ 25°C unless otherwise specified)

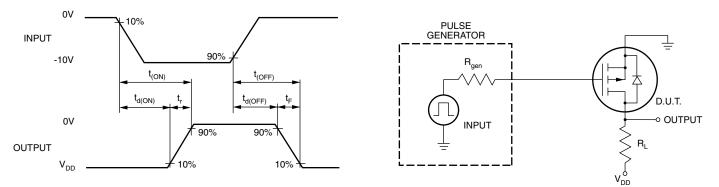
| Symbol | Parameter | Min | Тур | Max | Unit | Conditions | |
|---------------------|---|------|------|-------|-------|---|--|
| BV_{DSS} | Drain-to-Source Breakdown Voltage | -500 | | | V | $V_{GS} = 0V, I_D = -1mA$ | |
| V _{GS(th)} | Gate Threshold Voltage | -2.0 | | -4.5 | V | $V_{GS} = V_{DS}, I_D = -1mA$ | |
| $\Delta V_{GS(th)}$ | Change in $V_{\text{GS}(\text{th})}$ with Temperature | | 3.5 | 6 | mV/°C | $V_{GS} = V_{DS}, I_D = -1mA$ | |
| I _{GSS} | Gate Body Leakage | | | -100 | nA | $V_{GS} = \pm 20V, V_{DS} = 0V$ | |
| I _{DSS} | Zero Gate Voltage Drain Current | | | -10 | | $V_{GS} = 0V, V_{DS} = Max Rating$ | |
| | | | | -1000 | μΑ | $V_{GS} = 0V, V_{DS} = 0.8$ Max Rating $T_A = 125^{\circ}C$ | |
| I _{D(ON)} | ON-State Drain Current | | -90 | | mA | $V_{GS} = -5V, V_{DS} = -25V$ | |
| | | -100 | -240 | | | $V_{GS} = -10V, V_{DS} = -25V$ | |
| R _{DS(ON)} | Static Drain-to-Source ON-State Resistance | | 85 | | Ω | $V_{GS} = -5V, I_{D} = -5mA$ | |
| | | | 80 | 125 | | $V_{GS} = -10V, I_{D} = -10mA$ | |
| $\Delta R_{DS(ON)}$ | Change in $R_{DS(ON)}$ with Temperature | | 0.85 | | %/°C | $V_{GS} = -10V, I_{D} = -10mA$ | |
| G _{FS} | Forward Transconductance | 25 | 40 | | mប | $V_{DS} = -25V, I_{D} = -10mA$ | |
| C _{ISS} | Input Capacitance | | 40 | 70 | | | |
| C _{OSS} | Common Source Output Capacitance | | 10 | 20 | pF | $V_{GS} = 0V, V_{DS} = -25V$ f = 1 MHz | |
| C _{RSS} | Reverse Transfer Capacitance | | 3 | 10 | | | |
| t _{d(ON)} | Turn-ON Delay Time | | 5 | 10 | | V _{DD} = -25V | |
| t _r | Rise Time | | 8 | 10 | ns | $I_D = -100$ mA R _{GEN} = 25 Ω | |
| t _{d(OFF)} | Turn-OFF Delay Time | | 8 | 15 | | | |
| t _f | Fall Time | | 5 | 16 | | | |
| V _{SD} | Diode Forward Voltage Drop | | -0.8 | -1.5 | V | V _{GS} = 0V, I _{SD} = -0.1A | |
| t _{rr} | Reverse Recovery Time | | 200 | | ns | V _{GS} = 0V, I _{SD} = -0.1A | |

Notes:

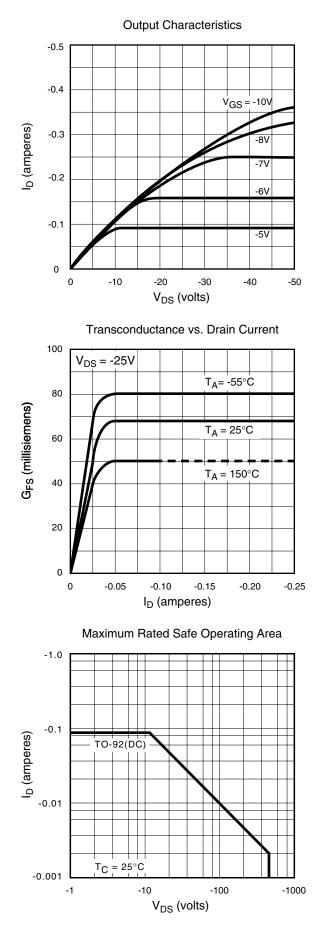
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

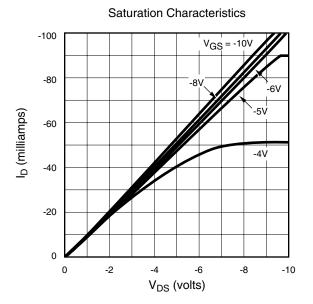
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

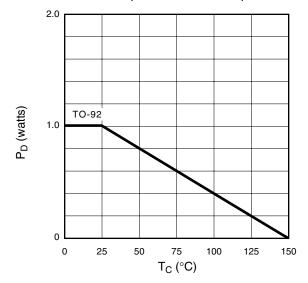


Typical Performance Curves

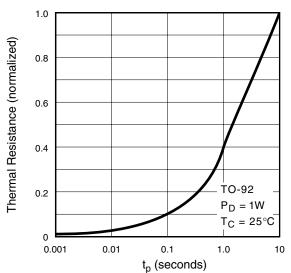




Power Dissipation vs. Case Temperature

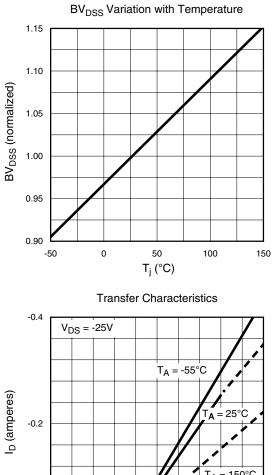


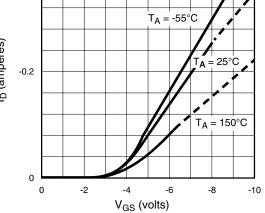
Thermal Response Characteristics



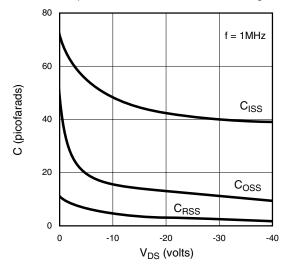
VP0550

Typical Performance Curves

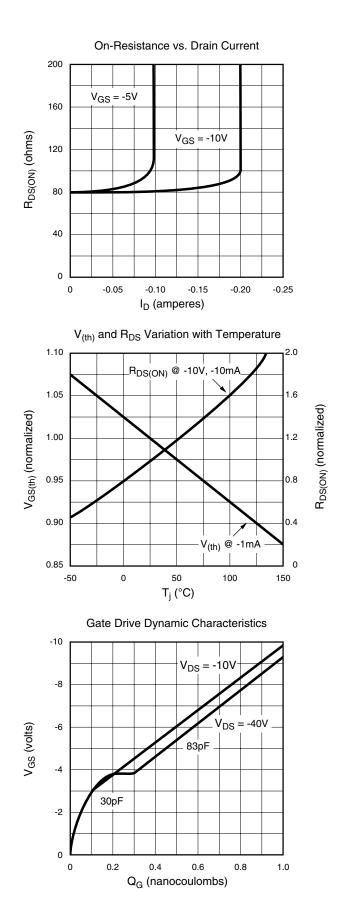




Capacitance vs. Drain-to-Source Voltage







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